US7729/09A

Hardware Architecture Reference Platform

User's Manual

HITACHI

US7729-HCB1/10/11 & US7709A-HCB1/10/11
US7729-HRP10A & US7709A-HRP10A
US7729-HRP11A & US7709A-HRP11A

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Read Me First

If you do nothing else please review sections 2 and 3 before you start. This will reduce the initial startup problems that may occur.

This document, as well as the hardware, is constantly being improved. Check with your technical support person periodically for available updates.

A simple diagnostic monitor program, primarily written in C language and referred to as CMON, is available “as is” and at no charge after completing and returning a release form. The form may be packaged with your new HARP, or supplied by a Hitachi sales representative.

Revision History

Rev	Date	Description
A.1	May 29, 2001	-Added Revision History -Corrected BSC Register Values in Appendix D -Fixed Minor Formatting Throughout Document -Fixed Minor Grammatical Errors
A.2	July 13, 2001	-Added Quick Start Guide for VxWorks

Section 1 Overview

1.1 Introduction

The Hitachi SuperH [tm] microprocessor-based Hardware Architecture Reference Platform (HARP) consists of a printed circuit board (PCB) or board set, schematics, sample software device driver source code, CPLD code, gerber files, bill of materials, and documentation. The schematics, sample software device driver source code, OEM abstraction layer (OAL) code, CPLD code, and gerber files are available to customers who complete a release form inside the original shipping box or available from a Hitachi sales representative.

The HARP serves as a complete, tested development platform and functional design that customers may incorporate all or part there of into their own end product. Generally, the HARP system ships as a two-board set: a base board with SH3 (SH770X), SH3-DSP (SH772X) microprocessor, SDRAM, flash memory, serial port, Ethernet connection, and expansion bus connector. JTAG emulator connector, CompactPCI interface. A daughter board (Tahoe) offers more functional capability. The HARP offers flexibility through board-to-board connectors allowing future HARPs to ship as one base board or a base board plus multiple daughter boards.

Several operating systems with sample device driver software or operating system board support packages run on the HARP. Operating systems running on or planning to run on the HARP include Microsoft's Windows CE, Wind River Systems' VxWorks and Tornado, OSSL's QNX, Linux, and Accelerated Technologies' Nucleus+. Check with Hitachi for a current list of suppliers and specific HARP system.

Hitachi offers the HARP as a stand-alone development board (SDB). A third party offers a chassis with CompactPCI backplane and built-in power supply. The chassis is known as the HARP case.

Optional development tools can be purchased from Hitachi and third-party suppliers. These tools include Hitachi's E10A emulator, Hitachi's Debugging Interface (HDI), and Agilent's logic analyzer.

1.2 Key West Base Board Features

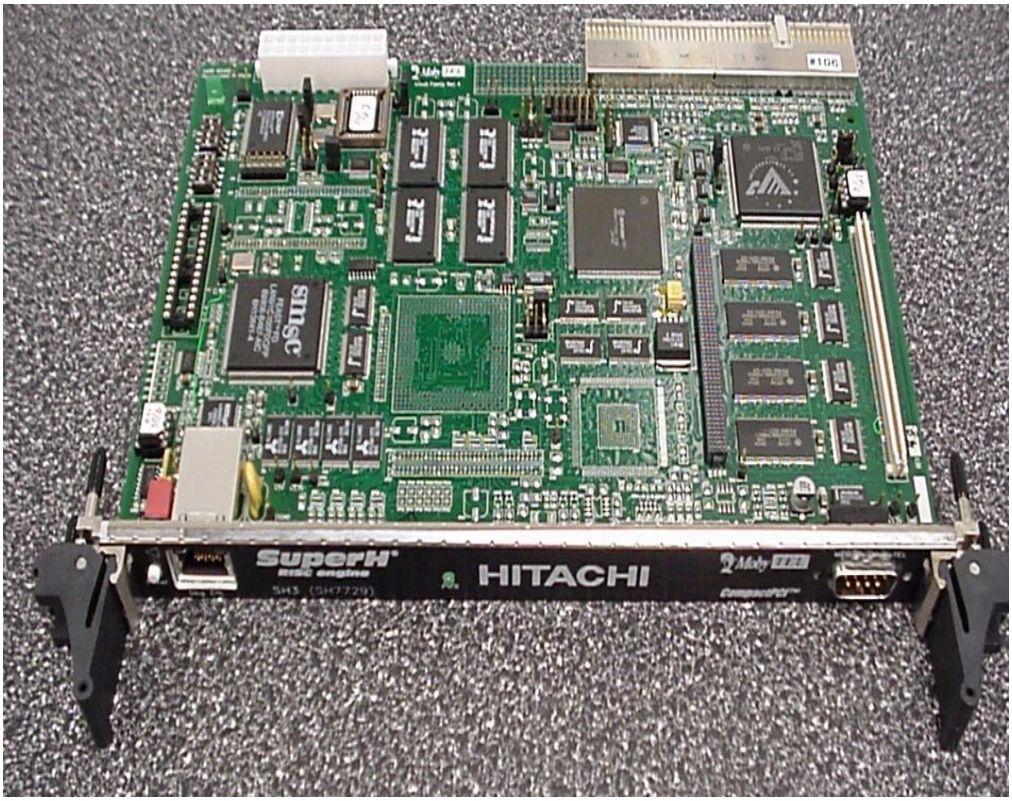


Figure 1.1 SH7709A/7729 Base Board (Key West)

- SH7709A/7729 processor running at 133 MHz (3.3 V)
- System bus: 32 bits wide running at 66 MHz
- 64 Mbytes of SDRAM for system memory
- 32 Mbytes of flash memory
- 10 Mbps and 100 Mbps 100BASE-T Ethernet (IEEE 802.3 compliant)
- Alphanumeric diagnostic LED display
- Pushbutton reset switch
- Full duplex RS232 COM serial port with flow-control for hardware/software debugging
- Two indicator LEDs for Ethernet: link, and TX/RX activity.
- One system LED (software controlled).
- Real-time clock
- 32-bit compact PCI interface supporting initiator (master) modes
- 200-pin SH bus connector
- 140-pin connector for plug-in daughter boards
- AutoPC connector for Microsoft's AutoPC daughter board (optional)

1.3 Tahoe Daughter Board Features

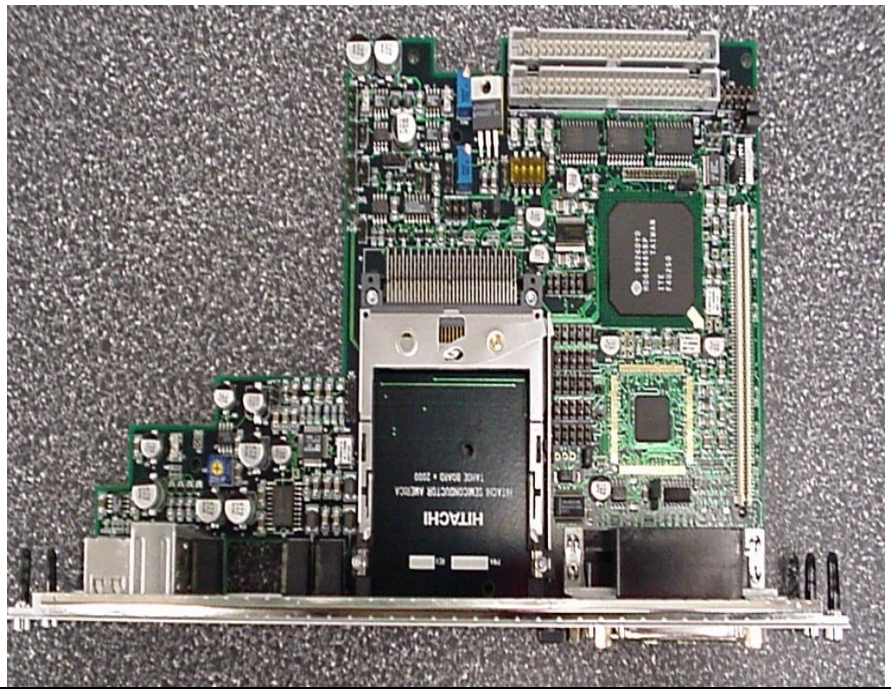


Figure 1.2 Tahoe I/O Board

HD64465

- PCMCIA interface that supports PCMCIA Rev. 2.1/JEIDA version 4.2 (2 slots)
- PS/2 keyboard interface
- PS/2 mouse interface
- IrDA (SIR – 115.2 kbps; FIR – through 4 mbps)
- USB host interface (2 ports)
- Touch screen 10 bit A/D interface
- AC97 audio codec interface
- AFE interface to modem
- Parallel port (1)
- Serial port (1)
- General purpose I/O ports

MQ200 Graphics Accelerator

- LCD/CRT interface

AD18 – AC97 Audio Codec

- Microphone in
- Audio in
- Stereo audio out

140-pin Expansion Connector

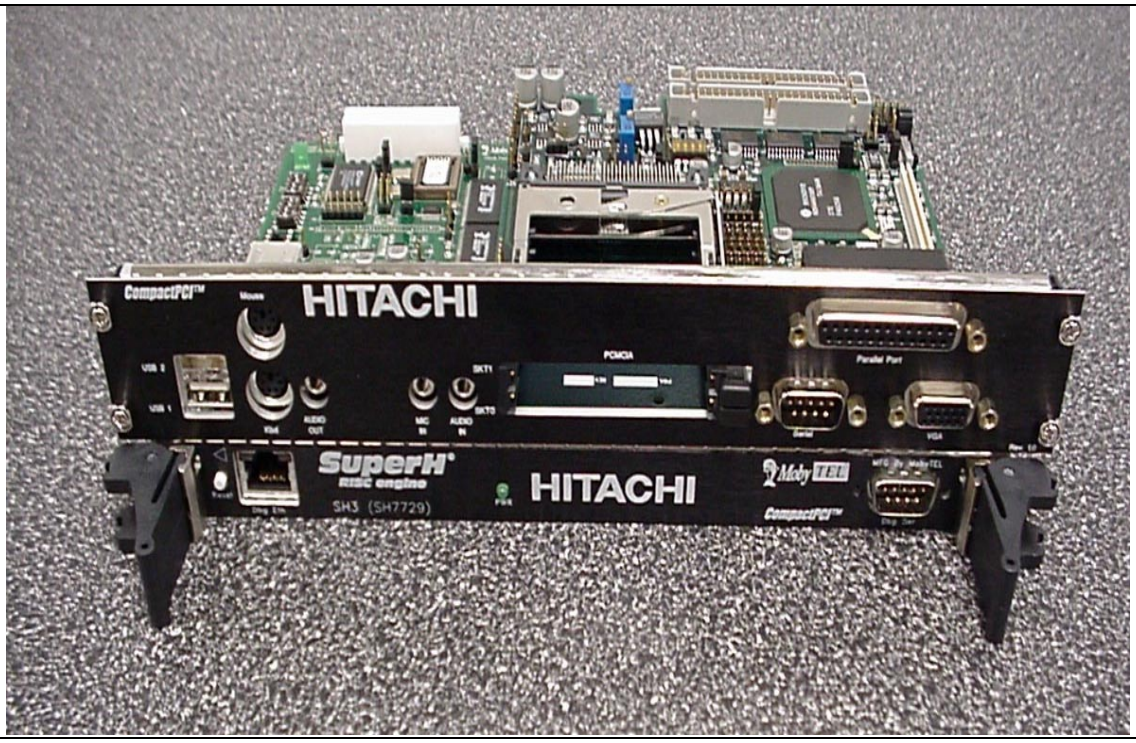


Figure 1.2 SH7709A/7729 HARP -- Key West + Tahoe

Section 2 Quick Start Guide (WinCE)

This section describes the following for the SH7709A/7729 HARP:

- The hardware and software requirements.
- Connections between a host system and the Key West.
- Downloading and running a binary image file.

2.1 System Requirements

2.1.1 Host PC Hardware and Software Requirements

The user supplies a host system with the following requirements:

- Hardware
  - CPU

  Pentium 133 MHz or greater recommended.
  - Memory

  32MB minimum, 64 MB or greater recommended.
  - Hard disk space

  Typical installation should require approximately 730 Mb.
  - CD ROM drive
  - Parallel Printer port

  Bi-directional (IEEE 1284)
  - RS-232 Serial ports

  One required, one optional
- Software
  - Microsoft Windows NT 4.0 service pack 3 or higher (service pack 5 for WinCE 2.12)
  - Microsoft Windows CE Platform Builder 2.12 or higher
- For application developers
  - Microsoft Visual Studio 6.0
  - Microsoft Windows CE Toolkit for Visual C++ 6.0 or higher

2.1.2 SH7709A/7729 Platform Requirements

In addition to the host system, the following is needed for operating the HARP:

- Standard ATX power supply (or CompactPCI chassis and power supply)
- Microsoft compatible PS/2 mouse
- Microsoft compatible PS/2 keyboard
- Null modem serial cable
- 25-pin parallel cable (CEPC cable)
- VGA monitor and cable

2.1.3 Shipped with SH7709A/7729 HARP

- SH7709A/7729 base board (Key West) with face plate
- System I/O daughter board (Tahoe) with face plate
- Null modem serial cable
- Ethernet cable
- 25-pin parallel CEPC cable
- ATX power supply with AC cord

2.1.4 SH7709A/7729 HARP Default Settings

The current Key West boot monitor and device drivers initializes the hardware as follows:

- Debug serial channel: 38400 bps, 8N1 (8 data bits, No parity, 1 Stop bit, No flow control)

Jumper and switch settings for the boards are described below. For further information on the jumper functions, reference Sections 3.1.7, 4.2.2 and Appendices D & E.

On Key West board:

- Default setting of DIP switch S1 = ON OFF OFF OFF (Board will come up in Boot Monitor)*
- Default setting of DIP switch S2 = ON ON OFF OFF
- JP5 jumper pins 1 & 2, pin 3 open. Silkscreen triangle denotes pin 1
- JP6 jumper pins 1 & 2, pin 3 open. Silkscreen triangle denotes pin 1
- JP9 jumper present
- JP11 jumper present
- JP35 removed to allow PCMCIA operation (installed for CompactPCI, which disables PCMCIA)
- JP38 jumper present
- JP39 jumper pins 1 & 2, pin 3 open. Silkscreen triangle denotes pin 1
- JP41 jumper pins 2 & 3, pin 1 open. Silkscreen triangle denotes pin 1
- JP42 jumper pins 1 & 2, pin 3 open in rev 4.8 board. Silkscreen triangle denotes pin 1. This jumper is not present in rev 4.9 board.
- All other jumpers are left open by default

Jumpers on the Tahoe board:

- JP1 jumper pins 1 & 2, pin 3 open. Silkscreen triangle denotes pin 1.
- JP2 jumper present (for reference, this jumper not present if baseboard is an Aspen)
- JP11 jumper pins 1 & 2, pin 3 open. Silkscreen triangle denotes pin 1.
- JP13 jumper pins 2 & 3, pin 1 open. Silkscreen triangle denotes pin 1.
- JP14 jumper present (for reference, this jumper not present if baseboard is an Aspen)
- JP23 present (for IrDA).
- JP28 jumper pins 2 & 3, pin 1 open. Silkscreen triangle denotes pin 1 (for IrDA).
- JP31 jumper pins 2 & 3, pin 1 open. Silkscreen triangle denotes pin 1 (for IrDA).
- All other jumpers are left open by default

* For reference, if the user would like to boot into the WinCE OS installed in FLASH, switch S1 would be set to: OFF OFF OFF OFF

2.2 Harp Connections

2.2.1 Key West Connections

1. Plug in the ATX 20-pin block power terminal to J1.
2. Connect the serial cable from DB9 front panel connector labeled “Dbg Mfg” (J9) of the Key West board to the COM port of the host PC.

2.2.2 Tahoe Connections

1. Plug the Tahoe 140-pin connector into the Key West 140-pin connector using “spacer board”.
2. Plug the Tahoe board on top of the Key West board.
3. Connect a PS/2 mouse in the upper PS/2 socket labeled “Mouse” and a PS/2 keyboard in the lower socket labeled “Kbd”.
4. Attach a VGA monitor to the 15 pin VGA monitor connector labeled “VGA”.
5. Connect the 25-pin “D” parallel port connector, labeled “Parallel Port” to the host PC through the special WinCE 25-pin parallel cable.

2.3 Power Up Sequence

Switch on the ATX power supply. You should now see:

- Prompt appears on the serial terminal
- Green reset LED turns on until reset sequence is completed

Ensure that the terminal is configured as 38400/8/N/1/NoFlowControl.

Reset Sequence

Press the reset switch SW1 located near the corner of the board. The green LED display will sequence and the red alphanumeric LED displays initialization status.

2.4 Installation of Tools

2.4.1 Serial Terminal Emulator (Hyperterm)

Hyperterm ships with the Windows NT distribution. You do not need to install it separately. To communicate with Key West through the serial port, start Hyperterm as follows:

1. **Start->programs->accessories->hyperterm->hyperterminal**.
2. Enter a name for this connection (i.e., **WinCE_38K**).
3. Select the serial COM port number that is connected to the serial cable from Key West.
4. Select the settings
    - Bits per second: 38400

- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None

5. **File->Save**. Save these settings so that you don't have to enter them the next time.
6. Select "Disconnect" and "Connect" on the menu bar to force Hyperterm to use the new settings.

2.4.2 CESH (Windows CE Parallel Port Download Tool)

1. Install the Windows CE Toolkit. Enable the parallel port download option during the installation..
2. Set the parallel port mode on the HOST PC to "bi-directional" in the BIOS setup program (accessed upon system boot).

2.5 Downloading a Windows CE image

The image can be downloaded either through the HDI/E10A (Hitachi emulator) or through the parallel port. You should have two Windows CE images::

- Nk.bin: Windows CE binary file to be downloaded using the parallel port
- Nk.sre: S-record file that can be downloaded through HDI.

2.5.1 Parallel Download

1. Copy the Windows CE image file **nk.bin** to the **c:\wince\release** directory (or whatever directory you used to install Windows CE)
2. Click on:
   a. **Start->programs->Windows CE platform builder->SHx tools->Build Minshell for SH3**
   This opens up a DOS prompt window with the appropriate environment to download a Windows CE binary image
   b. C:\Wince211> **cd release**
   c. C:\Wince212\release> **cesh –s –p cepc**

   From the serial terminal program type the "load" command (lowercase L) at the prompt:
   FW> l

   Now you should see the image being downloaded through CESH. Wait until it finishes.
5. The image should start automatically after the download is complete.

2.6 Running Windows CE

You should see the Windows CE "splash" screen on Key West video display after the platform has booted up. You can try out the following commands from the Windows CE keyboard:

1. Alt-Tab
2. Click on Run.
3. Click on Browse.
4. Double click on **cmd.exe**.
3. Click OK.

4. The command prompt shell will appear on the display monitor.
5. Typing **dir <Enter>** will display a list of files and folders from Windows CE.

2.7 Tested Hardware

The following have been tested with the HARP WinCE platform:

- Microsoft Intellimouse PS/2 Mouse
- Logitech PS/2 Mouse
- Logitech USB Mouse
- Microsoft Natural Elite USB Keyboard
- SIIG Pocket Size 4 Port USB Hub

Section 3 Quick Start Guide (VxWorks)

The following information gives guidelines and suggestions for the setup of the SH7751 HARP when using the Wind River Tornado tools. The *Wind River Tornado User's Guide* was used as a guide for some of the explanation and can be referenced for a more complete guide for the installation.

3.1 Installing Tornado 2 on a Windows Host PC

There are a number of ways to set up Tornado 2 with the different platforms. This section will discuss the Windows environment. Before beginning the installation, you should have administrative privileges on the host PC. Without administrative privileges, you will not be able to install Tornado 2 for all users.

1. Insert the Tornado 2 CD-ROM into the Host PC's CD-ROM drive.
2. The SETUP program should "autorun" and you should see the "Welcome" window. If not, manually run `D:\SETUP`, where "D" represents the drive letter of the CD-ROM drive.
3. At the "Welcome" window, click the "**Next>**" button to continue.
4. The "`README.TXT`" document is displayed. After reading the latest release notes, click the "**Next>**" button.
5. The "License Agreement" window appears. Read the License Agreement and click the "**I Accept**" button. Now, you may click the "**Next>**" button to continue.
6. At this point, you may receive a warning if you do not have administrative privileges. You may continue by clicking the "**Next>**" button or you may cancel the installation by clicking the "**Cancel**" button.
7. In the "User Registration" window, enter the appropriate information for the "Name," "Company," and "Key" fields. The "Key" field refers to the CD-key that came with that particular disc. Take care when entering the key; it is case-sensitive. When all of the fields are complete, click the "**Next>**" button.
8. At the "Installation Options" window, choose a full install by selecting the "Full Install" option. Click the "**Next>**" button to continue.
9. In the "Project Information" window, enter the name of the project and the number of licensed users in the appropriate fields. In many cases, these values can be virtually anything. Click the "**Next>**" button.
10. The "Select Directory" window will appear. Here, select a location to install Tornado 2. Enter the location in the "Destination Director" field. Click the "**Next>**" button to continue. If the selected directory does not exist, a prompt will appear asking for permission to create it. In this document, we will assume that the directory is `C:\Tornado`.
11. In the "Select Products" window, you may select the individual components to be installed. By default, all ordered products are pre-selected. Make sure that there is an adequate amount of free disk space. Click the "**Next>**" button to continue.
12. The "Select Folder" window appears. Here, enter the program folder in which SETUP will create shortcuts to the installed components of Tornado 2. From here, we will assume that the default value, "Tornado2" is accepted. Click the "**Next>**" button to accept your selection.
13. At the "Tornado Registry" window, select an option that best suits individual needs. Although mostly unaffected by your choice, the instructions presented here will assume that the Tornado Registry is installed locally in the startup group. Click the "**Next>**" button to continue.
14. The "Backward Compatibility" window will appear. Select "no" and click the "**Next>**" button to begin installation. This is the last window before SETUP begins copying files.
15. The file copy procedure may take a significant amount of time to complete. Depending on the size of your installation and the speed of the host PC, it may take anywhere from several minutes to several hours to complete.
16. When the procedure is complete, the "Finish" window will appear with a list of successfully installed components. Click the "**OK**" button to complete the setup process and close SETUP.

3.2 Download BSP from Platform Support Site

1. Using a standard web browser, view the following page:
   http://ftp.hsa.hitachi.com/netshare/capp01/
2. There, you will find links to the BSP files. These will be labeled "**`Tornado 2.0`**" or "**`T2.`**" They are ZIP files and are named in this manner: **`aspen_t2.zip`**; **`bigsur_t2.zip`**; **`keywest_t2.zip`**
3. Download the **`keywest_t2.zip`** file.
4. Create a new directory for the BSP: `C:\Tornado\target\config\KeyWest\`
5. Using a compression utility, extract all of the files from the ZIP archive to the newly created directory: `C:\Tornado\target\config\KeyWest\`.
6. In that directory, you will need to create a makefile. Depending on the endian setting of the target, copy either the "**`MakeBigEndian`**" file or the "**`MakeLittleEndian`**" file. Paste the file into the same directory, and re-name it "**`MakeFile`**."

3.3 Modify config.h

This step is optional. This procedure edits the default settings in the `config.h` file before building the `bootrom.hex` file, thereby eliminating the need to enter the same information after every reset of the target.

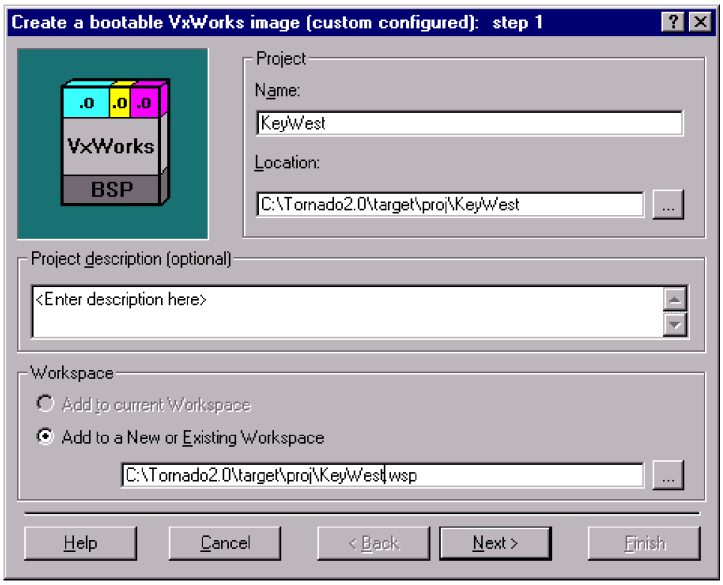
1. Edit the `config.h` file with any text editor. Look for something similar to the following lines:

   ```
   #define DEFAULT_BOOT_LINE \
   "fsmc(0,0)SJ2-KKIM:D:\\proj\\aspenLE\\default\\vxWorks h=137.168.149.119 e=137.168.149.235 u=kkim pw=190713 tn=target1"
   ```

2. Replace "SJ2-KKIM" with the host PC's name. This information can be found in the "Identification" tab of the Network Neighborhood Properties dialog of most versions of Windows. Just right-click "**Network Neighborhood**" on the desktop and click "**Properties**"
3. Replace "D:\\proj\\aspenLE\\default\\vxWorks" with the full path and filename of the VxWorks image file. Typically, this is: "C:\\tornado\\target\\proj\\KeyWest\\default\\VxWorks"
4. Enter the host PC's IP address after the "h=" string.
5. Enter the target's IP address after the "e=" string.
6. Enter a user name after the "u=" string.
7. Enter a password after the "pw=" string.
8. Enter the target's name after the "tn=" string.
9. Save the changes to the file.

3.4 Build VxWorks and Boot ROM Images

1. Make sure the Tornado Registry is running. You should see its icon in the Windows tray on the taskbar. If not, start it manually from the **Start→Programs→Tornado2→Registry** shortcut.
2. Start Tornado 2 from the start menu at **Start→Programs→Tornado2→Tornado**
3. The "Create Project in New/Existing Workspace" dialog window should appear upon startup. If it does not appear, select "**New Project**" from the "**File**" menu.
4. In the "New" tab, select "**Create a bootable VxWorks image (custom configured)**" and click the "**OK**" button.
5. The window "Create a bootable… …step 1" appears. Here, enter the project's name, location, and workspace. A sample diagram is shown below. After entering the relevant information, click the "**Next>**" button.



6. In the next window, "Create a bootable… …step2," Select the "**A BSP**" radio button. In the drop-down list, choose "KeyWest". Click the "**Next>**" button to continue.
7. A window will appear with your current selections. To finish creating the new project, click the "**Finish**" button. This will generate project dependencies.
8. When the process is complete, select "**Rebuild All**" from the "**Build**" menu. This will begin building the VxWorks image, which may take a few minutes to complete.
9. From the "**Build**" menu, select "**Build Boot ROM…**"
10. In the "Build Boot ROM" window, select "KeyWest". Select "bootrom.hex" as the image to build. When ready, click the "**OK**" button to begin building the boot ROM image.
11. If one does not exist, create a "`release`" subdirectory in the root directory (ex. "`C:\release\`"). Copy the `bootrom.hex` file from the `C:\tornado\target\config\KeyWest\` directory to this `C:\release\` directory.

3.5 Downloading "bootrom.hex" Image to the Target

There are several methods available to download images to the target. We will use DMON's "LE" command in conjunction with a TFTP server. Tftpd32 is a freeware TFTP server and is included in the support CD-ROM. It is also available for download on the Platform Support web page at http://ftp.hsa.hitachi.com/netshare/capp01/ as well as other locations on the Internet. Simply extract the ZIP file to a known location.

Setup TFTP Server

1. Start the TFTP server by executing `tftpd32.exe`. Click the "**Settings**" button to bring up the "Tftpd32: Settings" dialog. In the "**Base Directory**" field, enter "`c:\release\`" or the appropriate directory. Click the "**OK**" button to close the dialog.
2. The "`bootrom.hex`" file should appear in the listing when the "**Show Dir**" button is clicked.

Setup HyperTerminal

1. From the **Start→Programs→Tornado2** menu, select either **VxWorks COM1** or **VxWorks COM2** as appropriate.
2. This will execute HyperTerminal. By default it is connected at 9600bps. To change this, we will first need to disconnect. Select "**Disconnect**" from the "**Call**" menu.
3. Select "**Properties**" from the "**File**" menu. A dialog may appear asking you to confirm the modem/port selection. If so, click the "**OK**" button.
4. The properties dialog appears. In the "**Connect To**" tab, select the appropriate serial port ("COM1" or "COM2") in the "**Connect using**" field.
5. Click the "**Configure…**" button to configure the serial port properties.
6. In the serial port's properties dialog, select the following configuration:

Bits per second:	**57600**
Data bits:	**8**
Parity:	**None**
Stop bits:	**1**
Flow Control:	**None**

7. Click the "**OK**" button to close the serial port properties dialog.
8. Click the "**OK**" button to close the connection's properties dialog.
9. Select "**Call**" from the "**Call**" menu to reconnect with the new configuration.

Setup the Target

1. Attach the null modem serial cable (supplied) from the target to the host PC's serial port.
2. Attach an Ethernet network cable to the target. This can be from a network hub via a standard Ethernet cable, or from the host PC directly via a crossover cable.
3. Attach the power supply to the power connector of the target.
4. Ensure that the board is configured to boot from the boot ROM (SW1-1 ON) and that flash memory is not write-protected (SW1-3 OFF)
5. Turn on the power supply and verify that the DMON monitor has booted successfully. The debug hex display should read "**`READY ..`**" and a prompt should appear in the HyperTerminal window.
6. At the DMON prompt, type "**`le`**" and press the **`<Enter>`** key.
7. When prompted, assign a valid IP address to the target board. Press the **`<Enter>`** key.
8. When prompted, enter the IP address of the host PC. This information is displayed in the Tftpd32 window or can be obtained with the "**`ipconfig`**" command at the DOS/Windows command prompt.
9. When prompted, enter the filename of the image: "**`bootrom.hex`**" and press the **`<Enter>`** key.
10. After successfully loading the image, proceed with programming the flash memory. Type "**`p`**" at the prompt and press the **`<Enter>`** key. The procedure should be complete in just a few seconds.

3.6 Setup FTP Server

1. Start the FTP server from the **Start→Programs→Tornado2** menu.
2. Select "**Users/rights…**" from the "**Security**" menu to open the "**User / Rights Security Dialog**" dialog.
3. Click the "**New User…**" button. In the "**User Name:**" field, enter the same user name as in the `config.h` file from Section 2.2.3. Click the "**OK**" button when done.
4. Enter a new password and verify it. This should be the same as the password in the `config.h` file from Section 2.2.3. Click the "**OK**" button when done.
5. Now that a new user is created, enter "c:\" (or another appropriate drive letter) in the "**Home Directory:**" field.
6. Click the "**Done**" button to finish creating the new user.

3.7 Launch VxWorks

1. Turn off the target.
2. Set switch SW1-1 to the OFF position to boot from flash memory.
3. Turn on the target.
4. In the HyperTerminal window on the host PC, boot information should be displayed along with a message: "`Press any key to stop auto-boot...`" and a numeric countdown. The default parameters that were included in the `config.h` file will be used in the auto-boot sequence. If there is a need to modify the parameters, press any key to stop the auto-boot procedure. Otherwise, skip the next instruction.
5. Type "`p`" and press <Enter> to display the boot parameters. If changes need to be made, use the "`c`" command. When all of the parameters are correct, use the "@" command to start the boot process.
6. If all settings are correct, VxWorks should be downloaded and it will boot shortly after. Tornado commands can be used to verify the attachment of the target.

Section 4 Hardware Description

Functional Description

CPU

The Key West may be configured with either a Hitachi SH7709A or SH7729 SH3 processor. The processor internal speed runs at 133MHz and the bus speed at 66MHz. Internal CPU available peripherals include:

- 8 KByte cache
- Two A/D
- D/A
- Limited General Purpose I/O
- Two RS-232 ports
- DMA controller
- Smart Card Interface

In addition to the SH7709A/7729 processor the MQ-200 video chip and HD64465 companion chip is used for tightly coupled and integrated expansion.

The Hitachi SH7729 processor can also be substituted for the SH7709A, since it is pin compatible and a functional superset. The SH7729 includes an additional on-chip DSP processor.

CPU is hard-wired for “little endian” processing for Window CE but can be jumpered for “big endian” to support other operating systems.

RAM

The Key West contains 64 MB of SDRAM.

Flash Memory

The board supports 32 MB of flash memory. HARP requires a hardware provision determined by the setting of two of the switches that forces the system to power up and execute directly out of Flash. In this case Boot PROM is ignored.

The Processor can block erase, and block-protect the Flash at a granularity finer than 1 MB/block. The processor is only able to write to flash memory only while executing out of Boot PROM.

There is a software controlled, global write protect register bit. This bit prevents the hardware from asserting the write-enable signal thus disabling all writes to flash memory.

Boot PROM

A boot PROM handles board initialization, flash memory loading, diagnostics and testing. The boot ROM contains a flash loader that is capable of loading Windows CE into the operating system flash. The boot PROM circuitry supports a 512KB Flash EPROM.

Monitor code will reside in the Boot PROM. This monitor will use the serial debug port at a rate of 38.4 kbps (8 data bits, 1 stop bit, and no parity).

LED Status Indicator

- 1 green STATUS

The Green LED is mounted on the faceplate. After power-on, the LED will be forced on by reset. As soon as the CPU comes out of reset the LED is turned off by software, indicating successful fetch of the first instructions. When Windows CE is running, the kernel will periodically toggle the LED, indicating normal operation.

Reset Button

Key West has a push button reset located on the faceplate.

Pushing this button has the exact same effect as an assertion of PRST# on the CPCI bus.

The system is forced into a hard-reset state whenever this button is pushed or PRST# is asserted. Releasing this button asserts PRST# which resets the HARP performs a cold reboot. All PCI reset requirements on RST# are satisfied when the PRST# signal is asserted.

Switches

There are two sets of DIP (dual in-line parallel) switches on Key West. Each set of DIP switches contains four switches. The first switch, S1, is requred by the Microsoft HARP specification and determines the operation of the HARP at power-on/reset time. The second set of switches, S2, is used by the monitor to select self-test functions. Both switches are readable by the processor.

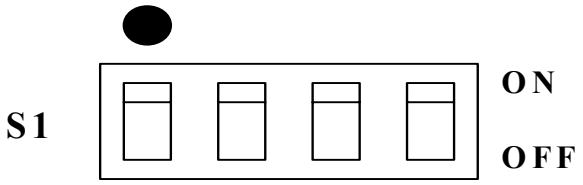


Figure 1 Switch Placement

Switch 1-1 is located under the dot, switch 1-2 is to the right of that, and switch 3 is to the right of that, and switch 4 is farthest to the right. The switch is considered on when it is pulled up towards the dot and off when it is pulled down.

Table 1: Switch S1 Settings

S1-1	S1-2	S1-3	S1-4	Function
ON	X	X	X	Code executes from the boot PROM following reset, and communication is over the debug serial port.
OFF	ON	X	X	Code starts executing from system Flash after reset. The debug serial port is used for debug communication.
OFF	OFF	X	X	Code starts executing from system Flash after reset. The debug Ethernet port is used for debug communication.
X	X	ON	X	The block write protection for the system Flash is enabled. Protected blocks cannot be written.
X	X	OFF	X	The block write protection for the system Flash is disabled. Protected blocks can be written.
X	X	X	ON	Bootloader will read switch, download image and jump directly to image
X	X	X	OFF	Bootloader will read switch go into monitor mode over Debug Serial Port link

Debug Serial Port

A serial port on the SH7709A/7729 processor is used as the debut RS-232 port. This port is available externally on the front panel as a DB9 connector.

The default baud rate of this port is 38.4 kbps. The port uses a male DB9 connector, identical in pin-out to a standard PC.

Table 2: Debug Serial Port Pin-out

Pin	Name		Pin	Name
1	DBG_CD		6	DBG_DSR
2	DBG_RX		7	DBG_RTS
3	DBG_TX		8	DBG_CTS
4	DBG_DTR		9	DBG_RI
5	GND			

This serial port (DBG_RX, DBG_TX) supports a serial data format of 8data, 1 stop and no parity.

The output signals DBG_DTR and DBG_RTS are directly controllable via register bits. The input signals, DBG_CD, DBG_DSR, DBG_RI, and DBG_CTS are visible as register bits.

Compact PCI Interface

The Compact PCI interface is implemented using the V3 Semiconductor V320 Bridge Chip. It supports both master and slave modes.

CompactPCI connects to the back-plane using CPCI connectors J1 and J2 (which map to the board connectors J11 and J7, respectively).

The CompactPCI system slot supports clock generation and arbitration. It also supports seven REQ/GRANT pairs and seven clock sets.

Key West complies with CompactPCI PCIMG 2.0 Revision 2.1, which is an extension of PCI specification version 2.1 and meets all PCI timing requirements for 33Mhz operation. It also meets the requirements for a universal 3.3V/5V card.

Note: Normally the PCI interface uses memory areas 5 and 6, which provides a 128 Mbyte memory space. Jumper J35 must be installed in order for PCI to use these memory areas. PCMCIA also uses these memory spaces. If J35 is removed, PCMCIA uses areas 5 and 6 and PCI is either not used or uses a much smaller memory space within Area 2.

CompactPCI Extensions

Signals ENUM#, FAIL#, DEG#, CLK5 and CLK6 are supported.

An interrupt will be generated when ENUM# is asserted.

The power supply signal FAIL# will generate a reset.

The power supply signal DEG# will interrupt the CPU in order to prepare for loss of power.

Clocks

There is a 33-MHz external crystal for the CPU which, when coupled with the SH7709A/7729's on-chip PLLs and clock divide circuitry, determines the speed of operation. Setting the SH7709A/7729 mode pins determines CPU clock speed, bus clock speed, and peripheral speed.

The Key West board as shipped has the clock mode setting switch configured to Mode 7.

Clock Mode (MD2-0)	CPU Clock	CPU Bus Clock	CPU Peripheral Clock
7	2x (133 MHz)	1x (66 MHz)	0.5x (33 MHz)

The main clock CKIO (66 MHz) from the CPU goes to a QS5V993 clock driver chip for buffering. This clock driver drives the clock to the SDRAM and PCI blocks.

The RTC has a 32.768-kHz external crystal. This signal only connects to the CPU.

There is a 33-MHz external oscillator for the PCI clocks.

Bus Speed	Frequency
SDRAM	66 MHz
V3-PCI Bridge	66 MHz
SMSC Ethernet	66 MHz
I/O Expansion	66 MHz

Timers

The SH7709A/7729 and 64465 chips provide five hardware timers to support Windows CE and other operating system. Under Windows CE two of these timers are assigned for kernel tasks, while the other three are available for user tasks.

The Timer 1 on the SH7709A/7729 is assigned to periodically interrupt the CPU. This timer is capable of being programmed to generate periods from 1 millisecond (mS) to 100mS in 2 uS increments.

The current value (count) of the timer is readable during the interval between interrupts.

This timer has an accuracy of 0.72 µs and has a resolution of 0.72 µs with a system clock of 66MHz, CPU clock set at 133.333MHz, Peripheral clock divide of 6 and a timer clock pre-scale of 1/16.

Software can change the period of this timer, setting a different interrupt period for each interrupt event.

The SH7709A/7729 includes a built-in real time clock (RTC with an input clock rate of 16.384 kHz) capable of lasting an elapsed time of greater than one day. It is capable of generating an interrupt to the processor any time of day within 1 second of its programmed time.

Debug Ethernet Port

Key West supports a 10/100BaseT Ethernet in full or half duplex. An LED indicates the 10/100 rate, Full/Half duplex with Activity and Link status. The design is compliant with IEEE 802.3 100BASE-T specifications and flow control.

Frame Buffer memory supports 64 outstanding transmit and receive packets (128kB of memory).

Product RS-232 port

The HD64465 on the Tahoe board provides a full RS-232 connected to an external DB9 connector.

The HD64465 UART module is 16550 compatible. This module performs the serial to parallel conversion on received data, and parallel to serial conversion on transmitted data. Individually, it contains a programmable baud rate generator that is capable of dividing the input clock by a number from 1 to 65535; the data rate of each can also be programmed from 115.2K baud down to 50 baud. The character options are programmable for 1 start bit; 1, 1.5, or 2 stop bits; even, odd, stick or no parity; and privileged interrupts.

Features

- Programmable FIFO or character mode
- In FIFO mode 16-byte FIFO buffer on the transmitter and receiver
- The programmable Baud rate generator allows the division of input clock by 1 to 2^{16}-1 and generates internal 16X clock
- MODEM control function (CTS#, RTS#, DTR#, DSR#, RI#, DCD#)
- Fully programmable serial-interface characteristics:
- 5, 6, 7 or 8 bit characters
- Even, odd, forced 0/1 or no parity bit generation and detection
- 1 ½, or 2 stops bit generation
- Baud rate generation (DC to 115.2K baud)

- False start bit detection

VGA Graphics

The graphics controller supports the MediaQ MQ-200 companion chip. The controller provides up to 1280 x 768 (along with many other variations) along with LCD display support.

MQ-200 features:

- Support for 1,2,4,15 and 16 bits per pixel (bpp).
- Built-in 16Mb frame buffer for the MQ-200 video controller.
- Triple 256x8 color lookup table for 1,2,4 and 8 bpp.
- Supports 640x480(VGA) to 1024x768(XGA) with multiple refresh rates for CRT
- Supports XGA,SVGA,VGA for passive dual scan color LCD w/ 8,16, and 24 bit interfaces
- Supports XGA,SVGA,VGA for active matrix color LCD w/ 8,16, and 24 bit interfaces
- All options are software programmable

The Tahoe board contains a 15-pin DB15 female, PC-style video connector. This connector pin-out is the same as that used on commercial PCs today (see Table 3 below) are:

Table 3: VGA Pin-out

Pin	Name
1	RED
2	GREEN
3	BLUE
4	NC
5	GND
6	GND
7	GND
8	GND

Pin	Name
9	NC
10	GND
11	NC
12	NC
13	HSYNC
14	VSYNC
15	NC

PS/2 Keyboard

A PS/2 keyboard interface is provided by the HD64465 on the Tahoe board. It is implemented as a Register Interface peripheral and all protocols and timing conform to IBM-PC PS/2 specifications.

The connector is a 6 pin MiniDIN with the following pin-outs:

Table 4: Keyboard PS/2 Connector Pin-out

Pin	Name
1	KBDAT
2	NC
3	GND

Pin	Name
4	VCC
5	KBCLK
6	NC

Parallel Printer Port

A parallel printer port is provided from the HD66465 on the Tahoe board. The parallel port uses a standard female DB25 form factor parallel port connector. The HD64465 companion chip provides the parallel port. WinCE 2.11 and 2.12 only supports this port as a debug Parallel Port- it is not available as a LPT-type port.

Also note that this is a host-configured port, similar to a PC parallel port. For a parallel port download this port needs to be connected to a host PC port. To support this host-to-host

configuration a special parallel port cable must be used. This cable can be obtained from Redmond Cable Corp., in Redmond, WA, PN MIC-64355913 (10 ft.), described as "CE/PE Parallel Cable, DB25M to DB25M."

Table 5: Parallel Port Pin-out

Pin	Name
1	NSTB
2	PPD0
3	PPD1
4	PPD2
5	PPD3
6	PPD4
7	PPD5
8	PPD6
9	PPD7
10	NACK
11	BUSY
12	PE
13	SEL

Pin	Name
14	NAFD
15	NERROR
16	NINIT
17	NSELIN
18	GND
19	GND
20	GND
21	GND
22	GND
23	GND
24	GND
25	GND

IrDA Serial Interface

The IrDA 1.1 capable serial port of the HD64465 companion chip is used to provide IrDA capability. A 10 pin IrDA standard connector is provided for use with an external IrDA transceiver and a board-mounted transducer is also provided. These are mounted on the Tahoe board.

The Fast IR (FIR) module is fully IrDA 1.1 compliant, and supports the serial infrared link at 288 Kbit, 576 Kbit, 1.152 Mbit and 4 Mbit. The three lower speeds comply with the Synchronous Data Link Control (SDLC) protocol (packets with start/stop flags delimiting a data packet encoded by zero-insertion). The 4 Mbit protocol uses an optical preamble and start/stop flags to delimit the 4 Pulse Position Modulated (4 PPM) packet data.

IrDA Features:

- Supports HP SIR or ASKIR infrared interface
- Supports FIR and MIR
- Provides DMA channel mode for FIR
- Supports STANDBY mode

This HARP board connector pin-out is shown below.

Table 6: IrDA connector Pin-out

Pin	Name	Direction	Function
1	TX	I	Transmit data
2	SEL1/ID1	I/O	I/O Pin for identification
3	GND	O	Ground
4	VCC	O	+5V or +3.3V
5	SEL2/ID2	I/O	I/O Pin for mode select and identification.
6	ID3	I/O	I/O Pin for identification
7	IRRX2	O	Receive data from FIR receiver.
8	RX1	O	Receive data from SIR if (SEL2 is low), or from demodulated 38KHz IR if SEL2 is high.
9	NC		
10	NC		

When the ID pins are in an input state they return an ID that indicates the type of IR "dongle" attached. The SDB has 100KΩ pull-up resistors (to VCC) on all of the identification (IDn) pins.

PS/2 Mouse Port

A PS/2 mouse interface is provided by the HD64465 on the Tahoe board. It is implemented as a Register Interface peripheral and all protocols and timing conform to IBM-PC PS/2 specifications.

The connector is a 6-pin Mini-DIN type and uses the standard PC pin-out shown below.

Table 7: Mouse PS/2 Connector Pin-out

Pin	Name
1	MDAT
2	NC
3	GND

Pin	Name
4	VCC
5	MCLK
6	NC

LCD Panel Support

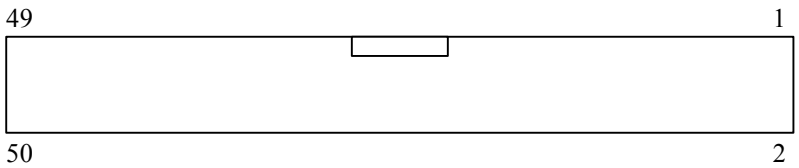
The MQ-200 video controller chip supports the LCD video output. There will be two default LCD headers available on Board 2, and the option to scramble the wire hookup to the second header if desired.

HARP LCD Header

The first header (JP33) is defined to meet the HARP LCD connector specification. It is a 50 pin connector, with the first 40 pins supporting the HARP specification. The connector uses a 0.1" spacing, ribbon cable style connector. Its pin-outs are noted below.

The 50-pin header is a 0.1" ribbon cable header, mounted on the Tahoe board. The top view of the header pin order is:

Figure 2: HARP LCD Connector pin-out



The second header (JP35) is a custom LCD connector. Contact Hitachi if more information is required.

Table 8 HARP LCD Header Signal Definitions

Name	Function
DF	The DF signal is used on some LCD panels for internal biasing. It is a clocking signal that changes state at the beginning of each new frame while the FRAME signal is active. During all even numbered frames it will be a '1' and during odd numbered frames it will be a '0'. An example of a panel that requires this signal is the Sharp LM48014F where the datasheet refers to the signal as M. The implementation of this signal is not required. If this signal is not implemented, it should be a "no connect".
ENABKL	Enable Back-light, H = On, L = Off
ENAVDD	Enable VDD supply on LCD panel, H = On, L = Off
ENAVEE	Enable VEE supply on LCD panel, H = On, L = Off
P0-23	LCD Data
FRAME	LCD Start of Frame signal. High pulse at start of each LCD frame.
LOAD	LCD Start of Line signal. High pulse at start of each LCD line.
XLEFT	Resistive touch panel X-Left conductor.
XRIGHT	Resistive touch panel X-Right conductor.
YLEFT	Resistive touch panel Y-Upper conductor.
YRIGHT	Resistive touch panel Y-Lower conductor.
CP	LCD data "dot clock". High pulse for each data transfer.
V12V	DC Supply 12V +/-5%, 80 mA
V5V	DC Supply 5V +/- 5%, 2A
V3V	DC Supply 3.3V +/- 5%, 2A
VSENSE	Binary indicator from panel to controller for preferred signal levels. H = 0V/5V. L = 0V/3.3V.

The voltage levels driven for signals P0-P15, CP, LOAD, FRAME, DF, ENAVEE, ENAVDD and ENABKL must be driven as indicated by the VSENSE pin. The VSENSE is pulled up with a 10KΩ resistor.

Table 9: HARP LCD Header Pin-out

1	VSENSE	2	V12V
3	ENABKL	4	GND
5	V3V	6	V3V
7	ENAVDD	8	V5V
9	V5V	10	ENAVEE
11	DF	12	GND
13	P0	14	P1
15	P2	16	P3
17	P8	18	P9
19	P10	20	P11
21	GND	22	P4
23	P5	24	P6
25	P7	26	P12
27	P13	28	P14
29	P15	30	GND
31	FRAME	32	LOAD
33	GND	34	CP
35	GND	36	XLEFT
37	XRIGHT	38	YUPPER
39	YLOWER	40	GND
41	P16	42	P17

43	P18
45	GND
47	P20
49	P22

44	P19
46	P21
48	P23
50	GND

Table 10: LCD Data Format

Data Pin	Citizen Color K6488L-FF 640x480 scan-line start	Citizen B/W G6485H-FF 640x480 Single Scan	Sharp Color LM8V30/1 640x480 scan-line start
P0	UD7 – Upper Scan Red 0	--	UD7 – Upper Scan Red 0
P1	UD6 – Upper Scan Green 0	--	UD6 – Upper Scan Green 0
P2	UD5 – Upper Scan Blue 0	--	UD5 – Upper Scan Blue 0
P3	UD4 – Upper Scan Red 1	--	UD4 – Upper Scan Red 1
P4	LD7 – Lower Scan Red 0	--	LD7 – Lower Scan Red 0
P5	LD6 – Lower Scan Green 0	--	LD6 – Lower Scan Green 0
P6	LD5 – Lower Scan Blue 0	--	LD5 – Lower Scan Blue 0
P7	LD4 – Lower Scan Red 1	--	LD4 – Lower Scan Red 1
P8	UD3 – Upper Scan Green 1	Pixel 0 (Upper leftmost)	UD3 – Upper Scan Green 1
P9	UD2 – Upper Scan Blue 1	Pixel 1	UD2 – Upper Scan Blue 1
P10	UD1 – Upper Scan Red 2	Pixel 2	UD1 – Upper Scan Red 2
P11	UD0 – Upper Scan Green 2	Pixel 3	UD0 – Upper Scan Green 2
P12	LD3 – Lower Scan Green 1	Pixel 4	LD3 – Lower Scan Green 1
P13	LD2 – Lower Scan Blue 1	Pixel 5	LD2 – Lower Scan Blue 1
P14	LD1 – Lower Scan Red 2	Pixel 6	LD1 – Lower Scan Red 2
P15	LD0 – Lower Scan Blue 2	Pixel 7	LD0 – Lower Scan Blue 2

The LCD panel must either allow the VSENSE pin to float or must drive it to ground in order to indicate the desired voltages for signaling panel. When the LCD panel grounds the VSENSE pin, the LCD controller must drive and receive the voltage levels 0V and 3.3V. When the LCD panel floats the VSENSE pin, the LCD controller must drive and receive the voltage levels 0V and 5V (4V minimum high voltage).

The signals P0-P15, LOAD, FRAME and CP will be source terminated with 22 Ohm resistors in series and 56Pf in parallel with the connector side of the resistor. Weak pull-down resistors should be added to ENAVEE, ENAVDD and ENABKL to insure that the panel remains off during power-on.

PCMCIA

The Tahoe board contains two PCMCIA slots that are supported by the HD64465 companion chip. Slot 0 of the double-high PCMCIA connector is located on the bottom and slot 1 is on top of slot 0.

The PC Card Controller (PCC) controls the internal buffers, interrupts, and PCMCIA-defined ports of the PC card interfaces, which is connected to the Intelligent Peripheral Controller (IPC). The PCC enables two slots of the PC cards that are compliant with the PCMCIA PC Card Specification Release 2.1 and JEIDA Version 4.2

Features:

- Two channels of the PC card interfaces can be simultaneously controlled
- Supports memory card interface, and I/O and Memory card interface, which function as PC card interfaces and are connected to physical memory areas 5 and 6.
- Area 6 is allocated to PC Card Channel 0 (PCC0) and supports memory and I/O interfaces.

- Area 5 is allocated to PC Card Channel 1 (PCC1) and supports both memory and I/O interfaces.

The ability to switch between Attribute memory or a Common memory, and I/O space is determined by the memory addressed by the CPU..

Note that there is an overlap of memory space for the PCI apertures and the PCMCIA socket. Via a two jumpers on the board, the user can select a PCI or PCMCIA aperture for address Areas 5 or 6.

Jumper J35 must be removed from the Key West board in order to use the PCMCIA sockets. If J35 is installed Area 5 and 6 can be used by the PCI interface and PCMCIA function is disabled.

USB

This USB Host Controller is a PCI-like implementation of the Universal Serial Bus (USB) 1.1 specification utilizing the OpenHCI. It contains an integrated Root Hub with two host USB ports, PCI-like interface, and USB Host Controller. The HD64465 companion chip on the Tahoe board provides the USB interface and has the following features:

- Supports 2 USB ports
- Supports device bandwidth of 12Mbps or 1.5Mbps
- Supports power management mode to protect USB Bus power; and over-current detector to protect USB Bus from abnormal over-current load
- Fully compatible with the USB specification version 1.1 and register compatible with Open HCI specification version v1.0 supported by Microsoft, Compaq and National Semiconductor.
- Internal 4 K-byte SRAM provided for USB Open Host Controller driver to store frame lists, transaction descriptors for USB host controller's schedule control and this internal memory is also used as data buffer for host controller to send/receive data to/from USB devices

For more information on the USB function, refer to the following references:

"USB Specification", Version 1.1

"OpenHCI Specification", Version 1.0

"PCI Specification", Version 2.1

Sound System

The Tahoe board contains an AC97 compatible sound chip capable of recording and playing back sounds and is supported by the HD64465 companion chip. A microphone connector is supplied for the recording of sounds. In addition a PC style stereo output jack is provided for connection to optional external speakers. Volume control and mute is under software control. No mechanical volume or mute controls are provided.

The sound system uses the digital protocol support of the HD64465 companion chip coupled with an external codec, the AC97.

Features:

- Directly interfaced to AC97 Codec for controlling voice data to the speaker, or from the microphone.
- Full-duplex data transfer between CODEC and this interface
- Dual TX/RX FIFO (8 x 32 -bit) are supported
- Voice captures and playbacks can be supported by SH7709A/7729 PIO/DMA mode access.
- Supports STANDBY mode

Auto PC Connector (factory installed option)

Microsoft has a reference platform that is used for running Windows CE inside an automobile called Auto PC. It consists of a CPU and a support card attached to a PCI bus.

A HARP Board may electrically connect to the Auto PC platform by adding an additional Molex connector (part number 52584-1209) to the CompactPCI bus. This connector is placed on the underside of the PCB and runs parallel to the board just in front of the CompactPCI connectors.

With the "A" side of the connector closest to the edge Compact Flash PCI connector, the pin out follows the standard PCI specification version 2.1.

Table 11: Auto PC Connector Pin-out

	A-Side
Pin	**Signal**
1	TRST
2	+12V
3	TMS
…	…
59	+5V
60	+5V

	B-Side
Pin	**Signal**
1	-12V
2	TCK
3	Ground
…	…
59	+5V
60	+5V

The Auto PC also requires the ability to wake up with any of eight low-true wake-up event interrupts.

Note: The Auto PC connector conflicts mechanically with CompactPCI application so only one option can be provided.

Hitachi 200 pin Local Bus Connector

Supports the 200 pin Hitachi Local Bus extender.

Hitachi 140 pin Local Bus Connector

Supports the 140 pin buffered local bus used to connect the Tahoe and other daughter boards.

Four Wire Touch screen input

A Four-Wire Touch Screen Input is supported by the HD64465. The drive control signals are provided by the **GPIO[3:1]** signals and the return A/D is supported by the **TSPX**,**TSMX**, **TSPY**, and **TSMY** signals.

All circuitry and support is provided on the Tahoe board.

Power Supply

Power to the Key West/Tahoe is supplied either through an ATX power connector in stand-alone mode, or by the CompactPCI chassis. Power supplied on the ATX connector is 3.3 V, +/-5 V, +/-12 V.

The SH7709A/7729 requires 1.8 V for the CPU core and 3.3 V for the I/O. The SDRAM runs at 3.3 V. The main CPLD runs at 3.3 V, the PCI, PCI arbiter, boot EPROM, and flash runs at 5.0 V. The compact PCI connector requires +/- 12 V.

Bus Interface

SDRAM Interface

Signal Name	Definition
CS3	Chip select for the 64 Mbytes of SDRAM
RAS3L/PTJ0	RAS for lower 32 Mbytes SDRAM
RAS3U/PTE2	RAS for upper 32 Mbytes SDRAM
CASLL/CAS/PTJ2	CAS for lower 32 Mbytes SDRAM
CASLH/CAS/PTJ3	CAS for upper 32 Mbytes SDRAM
CKE/PTK5	CKE for all SDRAM
R/W	Read/write for all SDRAM
WE[0:3]	Upper and lower DQMs for SDRAM
CKIO	Clock for all SDRAM

Note: The 100 MHz SDRAM parts will be used.

Ethernet Interface

The Ethernet interface is a standard 10Base-T implementation on an RJ45 connector.

RJ45 Pin	Signal	I/O
1	Tx+	Out
2	Tx-	Out
3	Rx+	In
4	—	—
5	—	—
6	Rx-	In
7	—	—
8	—	—

H-UDI Port Definition

The H-UDI port provides support for the Hitachi E10A emulator. The E10A is a software and hardware development support tool for applications using the SH7709A/7729.

I/O Port	Definition
TCK/PTF4/PINT12	H-UDI_TCK
TDI/PTF5/PINT13	H-UDI_TDI
TMS/PTF6/PINT14	H-UDI_TMS
TRST/PTF7/PINT15	H-UDI_TRST
TDO/PTE0	H-UDI_TDO
ASEBRKACK	ASEBRKACK
ASEMDO	ASEMDO (needs to be 0 to enable JTAG)

Section 5 Programmer's Guide

Memory Map

The SH7729 Key West Demonstration Platform is a stand-alone computing system. The SH3 MCU supports up to seven external chip select spaces: Boot Flash (EPROM), SDRAM, PCI, Ethernet, Parallel Port, PCMCIA, and daughter card interface. The flash-memory resource can be erased and reprogrammed in 64 Kbytes blocks and provides protection for bootstrap program storage.

The SH-3 processor has a fixed partition of address space. It supports six external 64MB segments or Areas in physical address space and one internal segment. The decode for these address areas is hard coded and available from the processor as six Chip Selects (CSn).

System Overview

Figure 3 : Overview of Address Space Assignments

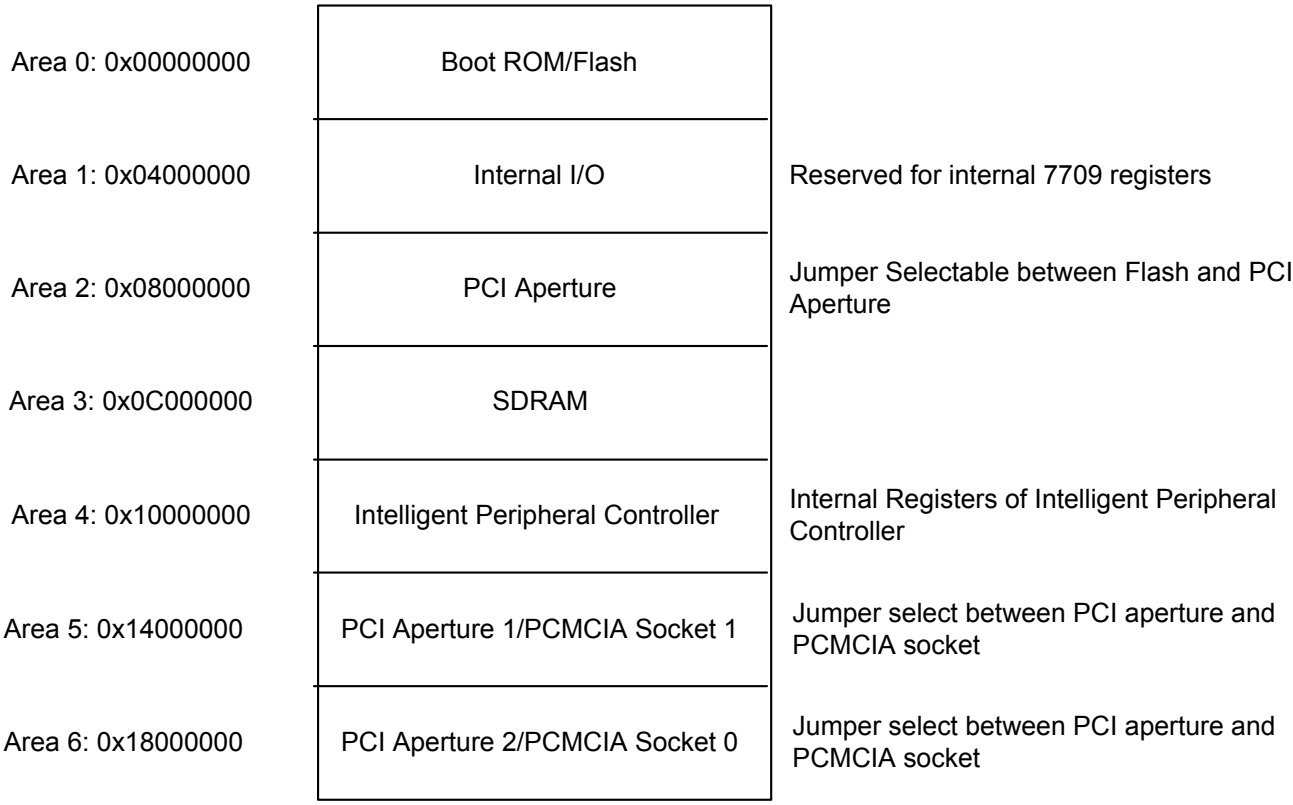


Table 12 System Address Space Definition

Area	Base Address	Upper Limit	Phys. Addr. A28-A26	Size	7709A/7729 Chip Select	Word Size*	Function

0	0x0000 0000	0x03FF FFFF	000	64MB	CS0	8 bit 32 bit	Boot ROM (512k x 8) or Flash (1M x 32 bit) with boot from Flash
1	0x0400 0000	0x07FF FFFF	001	64MB	None		Internal 7709A/7729 peripherals
2	0x0800 0000	0x0BFF FFFF	010	64MB	CS2	32 bit	PCI Aperture Flash with boot from Boot ROM
3	0x0C00 0000	0x0FFF FFFF	011	64MB	CS3	32 bit	SDRAM
4	0x1000 0000	0x13FF FFFF	100	64MB	CS4	32 bit	HD64465 decode: 32 bit I/O; Local USC registers; Diagnostic 8 digit Alpha display Ethernet registers and frame buffer CPLD option register V3 PCI Configuration Ports MQ200
5	0x1400 0000	0x17FF FFFF	101	64MB	CS5	32 bit	PCI Aperture 1/PCMCIA 1
6	0x1800 0000	0x1BFF FFFF	110	64MB	CS6	32 bit	PCI Aperture 2/PCMCIA 0
7	0x1C00 0000	0x1FFF FFFF	111	64MB			Reserved by Hitachi

* All data widths except Area 0 are set by internal registers. Area 0 is set by Mode pins MD3 and MD4, and is configured by S1-1.

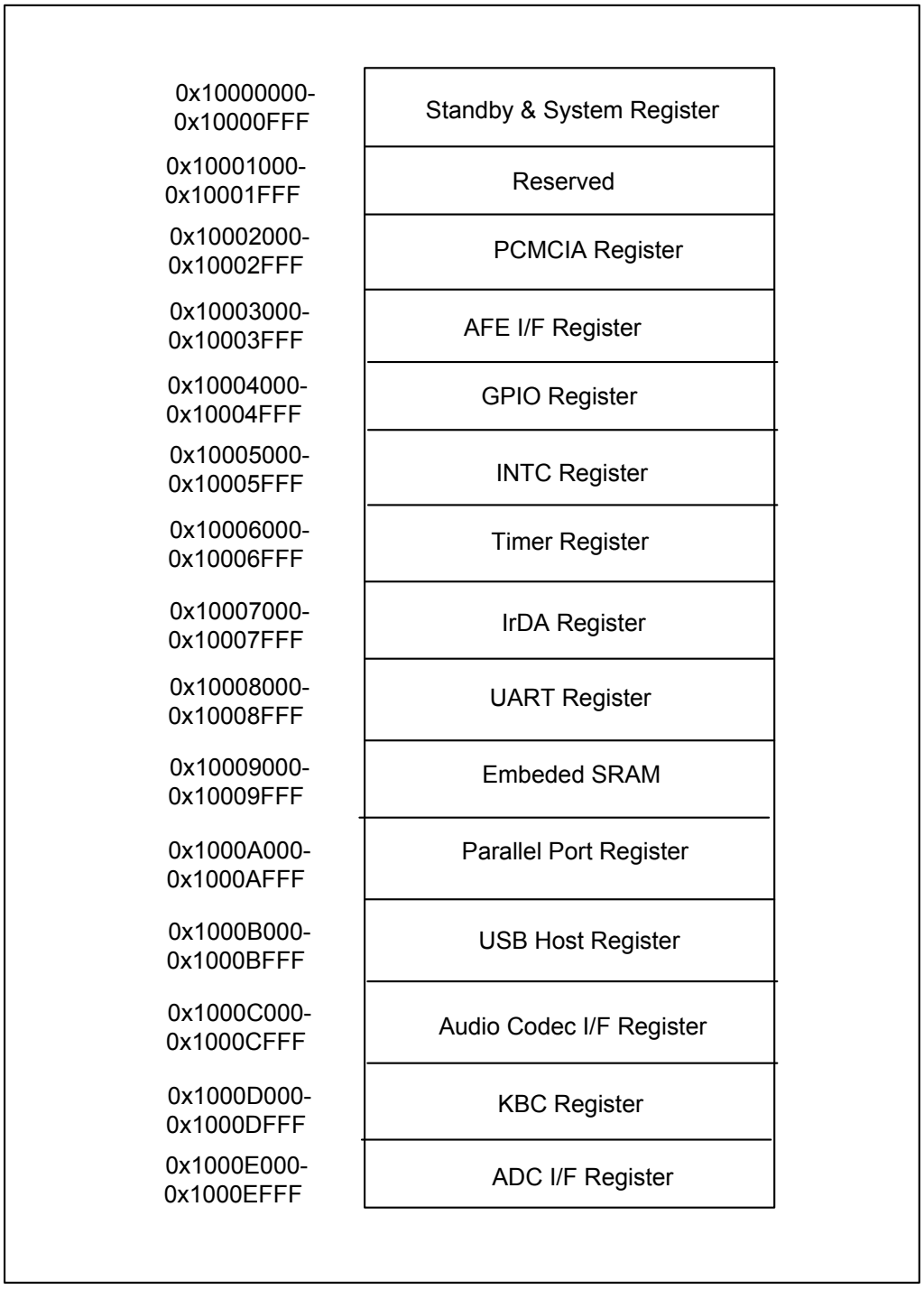
Ignored Address Bits: A31-A29

Shadow Offset to all addresses = 0x20000000*n where n=1 to 6

Address space Area 5 and 6 need special explanation. In both cases the address area supports two mutually exclusive functions, either a PCI aperture or PCMCIA sockets. Jumper (J35) selects whether the PCI aperture or the PCMCIA socket is selected for both areas.

HD64465 Memory Mapping, Area 4

Table 13: HD64465 Address Mapping



Miscellaneous Devices, Area 4:
V320USC PCI Configuration Ports
Base Address: 0x11FD 0000

See the V3 V320USC chip specification for further details of this register space.

Diagnostic Display (HP HDSP-2534)
Base Address: 0x11FF E000

See the HP HDSP-2534 device specification for further details of this register space. All functional aspects of this display are supported.

Special notes:

The Display is based on a byte address boundary but is in a 32 bit SH3 address space. The processor will always try to do 32 bit write but only D[7:0] will actually be written.

The display D[7:0] is mapped to the bus D[7:0].

Physical address A[4:0] is mapped to device address A[4:0]. FL# of the device is mapped to physical address A5.

Ethernet Device (SMSC LAN91C100FD & PHY LAN83C180)
Base Address: 0x11FE 0000

This device is mapped into a 32-bit SH3 data segment and all accesses are forced to a DWORD boundary.

See the SMSC LAN91C100FD document for specific decoding. Note that the Frame buffer memory (128KB), the PHY chip and the Ethernet EEPROM are all accessible via the register mapping of the LAN91C100FD.

CPLD Registers
External Bus/Board ID Register
Base Address: 0x11FF D000

Data Assignments (RO = Read-Only, RW = Read-Write):

D07	D06	D05	D04	D03	D02	D01	D00
N/A	N/A	N/A	EXT65BUS	EXT64BUS	BD_ID2	BD_ID1	BD_ID0
RO	RO	RO	RO	RO	RO	RO	RO
X	X	X	1	1	X	X	X

EXT65BUS: A “1” indicates that we are driving a HD64465 chip on the daughter board. A “0” indicates that we are driving a HD64465 on the main board.

EXT64BUS: A “1” indicates that we are driving a MQ200 chip on the daughter board. A “0” indicates that we are driving a MQ200 on the main board.

BD_ID[2:0]: These bits represent different versions of Hitachi daughter boards. At present there is no pull-up on these pins, so there is no guarantee of what state these pins will be if no external board is present. We should be able to test to see if an external board is present by reading this location, then writing the complementary value and then reading back the value. If no external board is present, we should be able to read back the complementary value.

Clock Select/LED0/PCMCIAEN Register
Base Address: 0x11FF C000

Data Assignments (RO = Read-Only, RW = Read-Write):

D07	D06	D05	D04	D03	D02	D01	D00
N/A	PCMCIA EN	LED0	N/A	N/A	SYSCLK SEL	PCICLK SEL	HD_CLK DIV2
RO	RO	RW	RO	RO	RO	RO	RO
X	0	X	X	X	X	X	X

PCMCIAEN: A “1” indicates that the PCMCIA decode is enabled for CS5 & CS6 address space. A “0” indicates that the PCI aperture decode is enabled for CS5 and CS6 and PCMCIA is not supported.

LED0: A “1” will turn on the endplate LED used to indicate power-up condition. A “0” will turn off that LED. This bit should power up in a “1” state. This bit is not available on a Rev 4 board.

SYSCLKSEL: A “1” indicates that we are running at full system bus speed, which in the typical case is 66MHz. A “0” indicates that we are running at ½ system bus clock speed.

PCICLKSEL: A “1” indicates that we are running at full system PCI bus speed, which in the typical case is 33MHz. A “0” indicates that we are running at ½ PCI bus clock speed.

HD_CLKDIV2: A “1” indicates that we are running the MQ200 and the HD64465 at ½ the clock speed of the rest of the system bus. A “0” indicates the hardware is running at the full system bus speed.

SW1 Register

Base Address: 0x11FF B000

Data Assignments (RO = Read-Only, RW = Read-Write):

D07	D06	D05	D04	D03	D02	D01	D00
N/A	N/A	N/A	N/A	MISCSW	FLASH PROT#	DEBUG SER#	BOOT PROM#
RO	RO	RO	RO	RO	RO	RO	RO
X	X	X	X	0	X	X	X

These bits output the value of the HARP designated Switch 1 (S1).

MISCSW: Used for general purpose SW control. Undefined at the moment.

FLASHPROT#: When “0” indicates that the FLASH can not be written to. A “1” indicates the FLASH can be written to.

DEBUGSER#: A “0” indicates that debug will be performed over the debug serial port. A “1” indicates that debug is done over the debug ethernet port.

BOOTPROM#: A “0” indicates that the system booted from the BOOT PROM versus the FLASH. A “1” indicates that the system booted from the FLASH.

Debug Register

Base Address: 0x11FF A000

Data Assignments (RO = Read-Only, RW = Read-Write):

D07	D06	D05	D04	D03	D02	D01	D00
N/A	DEBUG6	DEBUG5	DEBUG4	DEBUG3	DEBUG2	DEBUG1	DEBUG0
RW	RW	RW	RW	RW	RW	RW	RW
X	X	X	X	X	X	X	X

This port is available for debug purposes to support any boot time self-test.

Board Type Register

Base Address: 0x11FF 9000

Data Assignments (RO = Read-Only, RW = Read-Write):

D07	D06	D05	D04	D03	D02	D01	D00
N/A	N/A	N/A	N/A	TYPE3	TYPE2	TYPE1	TYPE0
RO	RO	RO	RO	RO	RO	RO	RO
X	X	X	X	X	X	X	X

TYPE[3:0] is the board type assigned to a design.

The list of presently assigned boards are:

TYPE[6:0]	Board Definition	Notes
1	H300/325/350/375b	7709/7729A processor

Board Revision Register

Base Address: 0x11FF 8000

Data Assignments (RO = Read-Only, RW = Read-Write):

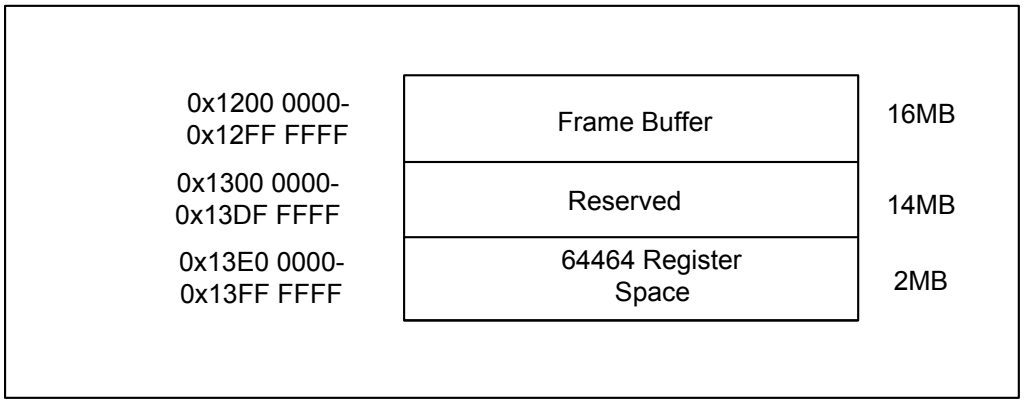
D07	D06	D05	D04	D03	D02	D01	D00
N/A	N/A	N/A	N/A	REV3	REV2	REV1	REV0
RO	RO	RO	RO	RO	RO	RO	RO
X	X	X	X	X	X	X	X

This register contains the revision level of the assembly. Presently existing revision levels are:

REV[3:0]	Notes
1	First Build
2	

MQ200 Memory Decode, Area 4:

Table 14: MQ-200 Address Mapping



See the MQ200 specification for further definition of these address spaces.

Functional Module	Address Range
Frame Buffer	0x1380 0000 – 0x139F FFFC
Reserved	0x13A0 0000 – 0x13DF FFFC
Power Management (PM registers)	0x13E0 0000 – 0x13E0 1FFC
CPU Interface (CC registers)	0x13E0 2000 – 0x13E0 3FFC
Memory Interface (MM registers)	0x13E0 4000 – 0x13E0 5FFC
Reserved	0x13E0 6000 – 0x13E1 3FFC
Interrupt Controller (IN registers)	0x13E1 4000 – 0x13E1 5FFC
PCI Configuration	0x13E1 6000 – 0x13E1 DFFC
Graphics Controller 1 & 2 (GC registers)	0x13E1 E000 – 0x13E1 FFFC
Graphics Engine (GE registers)	0x13E2 0000 – 0x13E2 1FFC
Flat Panel Controller (FP registers)	0x13E2 2000 – 0x13E2 3FFC
Color Palette 1 (C1 registers)	0x13E2 4000 – 0x13E2 5FFC
Color Palette 2 (C2 registers)	0x13E2 6000 – 0x13E2 7FFC
Reserved	0x13E2 8000 – 0x13E2 9FFC
Device Configuration	0x13E2 A000 – 0x13E2 BFFC
Reserved	0x13E2 C000 – 0x13FF FFFC

Hardware Resource Assignments

LED Status Indicators

Table 15: LED Status Indicator Port Assignments

LED	Color	Source	I/O Port	Notes
LED0	Green	7709A/7729		

A “1” indicates that the LED is on, and a “0” will turn the LED off.

Switch inputs

Table 16: Switch S1 Port assignments

Switch	SIGNAL	Target	I/O Port
S1-1	BOOTPROM#	7709A/7729	PTG0; Rev 4 Bd. or less only

S1-2	DEBUSERIAL#	7709A/7729	PTG1; Rev 4 Bd. or less only
S1-3	FLASHPROT#	7709A/7729	PTG2; Rev 4 Bd. or less only
S1-4	MISCSW	7709A/7729	PTG3; Rev 4 Bd. or less only
S1-1	BOOTPROM#	U6 – CPLD	See 0 above. Applies to Rev 5 Bd. and above
S1-2	DEBUSERIAL#	U6 – CPLD	See 0 above. Applies to Rev 5 Bd. and above
S1-3	FLASHPROT#	U6 – CPLD	See 0 above. Applies to Rev 5 Bd. and above
S1-4	MISCSW	U6 – CPLD	See 0 above. Applies to Rev 5 Bd. and above

MISCSW: A ON indicates that the System Boot Monitor should download automatically. An OFF indicates that the monitor should come up in command line mode (via the debug serial port). See SW2 below.

FLASHPROT#: When ON indicates that the FLASH can not be written to. A OFF indicates the FLASH can be written to.

DEBUGSER#: A ON indicates that debug will be performed over the debug serial port. A OFF indicates that debug is done over the debug Ethernet port.

BOOTPROM#: A ON indicates that the system booted from the BOOT PROM versus the FLASH.

Table 17: Switch S2 Settings

S2-1	S2-2	S2-3	S2-4	Definition
OFF	OFF	OFF	OFF	Reserved for future upgrades
OFF	OFF	OFF	ON	Lower 32MB SDRAM Test
OFF	OFF	ON	OFF	Upper 32MB SDRAM Test
OFF	OFF	ON	ON	Full SDRAM Test 1 through 6
OFF	ON	OFF	OFF	POST; Loop on Failure
OFF	ON	OFF	ON	POST; Indicate Failure and Continue
OFF	ON	ON	OFF	Reserved for future upgrades
OFF	ON	ON	ON	Display PCB Revision
ON	OFF	OFF	OFF	LED Test
ON	OFF	OFF	ON	Reserved for future upgrades
ON	OFF	ON	OFF	Reserved for future upgrades
ON	OFF	ON	ON	Reserved for future upgrades
ON	ON	OFF	OFF	Load Monitor; Automatic Ethernet Boot if S1 – 4 is ON
ON	ON	OFF	ON	Load Monitor; Automatic Serial Boot if S1 – 4 is ON
ON	ON	ON	OFF	Load Monitor; Automatic Parallel Boot if S1 – 4 is ON
ON	ON	ON	ON	Reserved for future upgrades

Switch 2 (S-2) is used to support debug and self-test modes for the system. They will primarily be used at Boot time.

Table 18: SDRAM 64MB tests

Test Number	Data Width	Test/Data Written
1	32 bit	Write Background of 0xFFFFFFFF and then walk through and read background, write foreground of 0x00000000, then read foreground
2	32 bit	Write Background of 0x00000000 and then walk through and read background, write foreground of 0xFFFFFFFF, then read foreground
3	32 bit	Write Background of 0xAAAAAAAA and then walk through and read background, write foreground of 0x55555555, then read foreground
4	32 bit	Write Background of 0x55555555 and then walk through and read background, write foreground of 0xAAAAAAAA, then read foreground
5	32 bit	Write Incrementing Address through memory. Then read memory and compare address
6	8 bit	Write Incrementing Address through memory (byte write). Then read memory and compare address (byte read).

Debug Serial Port

Table 19: Debug Serial Port Resource Assignment

Signal	Source	I/O Port	Notes
DTR2	7709A/7729	SCK1/SCPT3	
RXD2	7709A/7729	RXD2/SCPT4	
TXD2	7709A/7729	TXD2/SCPT4	
DSR2	7709A/7729	SCK2/SCPT5	
RTS2	7709A/7729	RTS2/SCPT6	
CTS2	7709A/7729	CTS2/IRQ5/SCPT7	
DCD2	7709A/7729	RAS2L/PTJ1	
RI2	7709A/7729	PTG4	R/O

Compact PCI Interface

The Compact PCI bus interface supports four standard bus interrupts A, B, C and D. Additionally we need to support two legacy ISA interrupts: INTP, and INTS. We need to support hot swap through a final interrupt, ENUM, which indications a board has been inserted or removed.

See Interrupt section 0 below, for further interrupt assignment information.

Table 20: CPCI Interrupt Assignments

Signal	Source	I/O Port	Notes
USC_INT#	7709A/7729	IRQ0/IRL0#/PTH0	IRQ0 mode; do not use this interrupt for the present revision
INTP	7709A/7729	PTC0/PINT0	PINT0 mode
INTS	7709A/7729	PTC1/PINT1	PINT1 mode
INTA#	7709A/7729	PTC2/PINT2	PINT2 mode
INTB#	7709A/7729	PTC3/PINT3	PINT3 mode
INTC#	7709A/7729	PTC4/PINT4	PINT4 mode
INTD#	7709A/7729	PTC5/PINT5	PINT5 mode
DEG#	7709A/7729	PTC6/PINT6	PINT6 mode
ENUM	7709A/7729	IRQ3#/IRL3#/PTH3	IRQ3 mode

Table 21: Special Read Byte Lane Control Resources

Signal	Source	I/O Port	Notes
RBEN#	7709A/7729	RAS2U/PTE1	PTE1 mode; output
RE0#	7709A/7729	CAS2H/PTE3	PTE3 mode; output
RE1#	7709A/7729	CAS2L/PTE6	PTE6 mode; output
RE2#	7709A/7729	CASHH/PTJ5	PTJ5 mode; output
RE3#	7709A/7729	CASHL/PTJ4	PTJ4 mode; output

Table 22: Bus Lockout control

Signal	Source	I/O Port	Notes
SH_IRQOUT#	7709A/7729	IRQOUT#	Setup mode so that signal will force external bus master (CPCI) to give up local bus

Timers

. The timer resources are in the 7709A/7729 and the HD64465 companion chip.

Product RS-232 Port

Table 23: Product Serial Port Resource Assignment

Signal	Source	I/O Port	Notes
URDTR	HD64465	DTR0	
URRXD	HD64465	RXD0	
URTXD	HD64465	TXD0	
URDSR	HD64465	DSR0	
URRTS	HD64465	RTS0	
URCTS	HD64465	CTS0	
URDCD	HD64465	DCD0	
URRI	HD64465	RI0	

IrDA Serial Interface

Table 24: IrDA Serial Interface Port Assignment

Signal	Source	I/O Port	Notes
IRDAMODSEL	HD64465	MODSEL/RX2	
IRDATXD	HD64465	TXD	
IRDARXD	HD64465	RX	
IRDAID1	HD64465	PD0	R/O
IRDAID2	HD64465	PD1	R/O
IRDAID2	HD64465	PD2	R/O

PS/2 Keyboard

The PS/2 keyboard support is used in the HD64465. Note that this is a PS/2 keyboard, not a scanned keyboard.

Table 25: PS/2 keyboard Port Assignments

Signal	Source	I/O Port	Notes
Keyboard Data	HD64465	KBDAT	
Keyboard Clock	HD64465	KBCK	

Parallel Printer Port

Table 26: Parallel Port Resource Assignment

Signal	Source	I/O Port	Notes
PP_STB#	HD64465	STB#	
PP_AFD#	HD64465	AFD#	
PP_ERR#	HD64465	ERR#	
PP_INIT#	HD64465	INIT#	
PP_SLIN#	HD64465	SLIN#	
PP_ACK#	HD64465	ACK#	

PP_BUSY	HD64465	BUSY	
PP_PE	HD64465	PE	
PP_SLCT	HD64465	SLCT	
PP_IPD[0..7]	HD64465	PPD[0..7]	

PS/2 Mouse Port

The PS/2 mouse support is used in the HD64465.

Table 27: PS/2 Mouse Port Assignments

Signal	Source	I/O Port	Notes
Mouse Data	HD64465	MSDAT	
Mouse Clock	HD64465	MSCK	

LCD Panel Support

Table 28: LCD Panel Resource Assignment

Signal	Source	I/O Port	Notes
FP_ENVDD	MQ-200	ENVDD	
FP_ENCTL	MQ-200	ENCTL	
FP_ENVEE	MQ-200	ENVEE	
FPDATA[0..23]	MQ-200	FD[0..23]	
FDE/FMOD	MQ-200	FDE/FMOD	
FP_FDI	MQ-200	FDI	
FPVSYNC	MQ-200	FVSYNC	
FPHSYNC	MQ-200	FHSYNC	
FPSCLK	MQ-200	FSCLK	
PWM0	MQ-200	PWM0	
PWM1	MQ-200	PWM1	

PCMCIA

Note that PCO is the physical lower socket (socket 0) and PC1 is the physical upper socket.

Jumper J35 must be removed to enable memory areas 5 and 6 for PCMCIA operation.

Table 29: PCMCIA Resource Assignment

Signal	Source	I/O Port	Notes
PC0CE1B	HD64465	PCC0CE1B#	
PC0CE2B	HD64465	PCC0CE2B#	
PC0RDB	HD64465	RDB#	
PC0WEB	HD64465	WEB#	
PC0IORDB	HD64465	PCC0ICIORDB#	
PC0IOWRB	HD64465	PCC0ICIOWRB#	
PC0RST	HD64465	PCC0RESET	
PC0WAIT	HD64465	PCC0WAIT#	

PC0WP	HD64465	PCC0WP#/IOIS16#	
PC0RDY	HD64465	PCC0RDY/IREQ0#	
PC0BVD1	HD64465	PCC0BVD1/STSCHG0#	
PC0BVD2	HD64465	PCC0BVD2/SPKR0	
PC0CD1	HD64465	PCC0CD1#	
PC0CD2	HD64465	PCC0CD2#	
PC0VS1	HD64465	PCC0VS1#	
PC0VS2	HD64465	PCC0VS2#	
PC0REG	HD64465	PCC0REG#	
PC0SEL0	HD64465	VCC0SEL0/CLOCK	
PC0SEL1	HD64465	VCC0SEL1/DATA	
PC0VPP1	HD64465	VCC0VPP1/LATCH	
	HD64465	VCC0VPP0	Not used
	HD64465	P8OLE	Not used
PC0D[0..15]	HD64465	PCC0D[0..15]	
PC0A[0..25]	HD64465	PCC0A[0..25]	
PC1CE1A	HD64465	PCC1CE1A#	
PC1CE2A	HD64465	PCC1CE2A#	
PC1RDA	HD64465	RDA#	
PC1WEA	HD64465	WEA#	
PC1IORDA	HD64465	PCC1ICIORDA#	
PC1IOWRA	HD64465	PCC1ICIOWRA#	
PC1RST	HD64465	PCC1RESET	
PC1WAIT	HD64465	PCC1WAIT	
PC1WP	HD64465	PCC1WP#/IOIS16#	
PC1RDY	HD64465	PCC1RDY/IREQ1#	
PC1BVD1	HD64465	PCC1BVD1/STSCHG1#	
PC1BVD2	HD64465	PCC1BVD2/SPKR1	
PC1CD1	HD64465	PCC1CD1#	
PC1CD2	HD64465	PCC1CD2#	
PC1VS1	HD64465	PCC1VS1#	
PC1VS2	HD64465	PCC1VS2#	
PC1REG	HD64465	PCC1REG#	
	HD64465	VCC1SEL0	Not used
	HD64465	VCC1SEL1	Not used
	HD64465	VCC1VPP1	Not used
	HD64465	VCC1VPP0	Not used
PC1D[0..15]	HD64465	PCC1D[0..15]	
PC1A[0..25]	HD64465	PCC1A[0..25]	

USB

These signals connect to the two stacked USB connectors on the Tahoe board.

Table 30: USB Resource Assignment

Signal	Source	I/O Port	Notes
USBPEN#	HD64465	USBPEN#	
USBOVR#	HD64465	USBOVR#	
USBD1P	HD64465	USBD1P	
USBD1M	HD64465	USBD1N	
USBD2P	HD64465	USBD2P	
USBD2M	HD64465	USBD2N	

AutoPC

AutoPC is typically not enabled.

Note that the AutoPC is in conflict with the E10 JTAG ports, so they are mutually exclusive.

Table 31: AutoPC Interrupt Resource Assignment

Signal	Source	I/O Port	Notes
AUTOINT0	7709A/7729	PINT8/PTF0	Active State Low; Uses PINT8 function
AUTOINT1	7709A/7729	PINT9/PTF1	Active State Low; Uses PINT9 function
AUTOINT2	7709A/7729	PINT10/PTF2	Active State Low; Uses PINT10 function
AUTOINT3	7709A/7729	PINT11/PTF3	Active State Low; Uses PINT11 function
AUTOINT4	7709A/7729	PINT12/PTF4/TCK	Active State Low; Uses PINT12 function; doubles as JTAG function
AUTOINT5	7709A/7729	PINT13/PTF5/TDI	Active State Low; Uses PINT13 function; doubles as JTAG function
AUTOINT6	7709A/7729	PINT14/PTF6/TMS	Active State Low; Uses PINT14 function; doubles as JTAG function
AUTOINT7	7709A/7729	PINT15/PTF7/TRST	Active State Low; Uses PINT15 function; doubles as JTAG function

Sound System

Table 32: Sound System Resource Assignment

Signal	Source	I/O Port	Notes
AD_ACCLK	HD64465	ACCLK	
AD_ACRST#	HD64465	ACRST#	
AD_ACPD#	HD64465	ACPD#/ACIRQ/PWE#	
AD_SIBDIN	HD64465	SIBDIN	
AD_SIBCLK	HD64465	SIBCLK	
AD_SIBDOUT	HD64465	SIBDOUT	
AD_SIBSYNC	HD64465	SIBSYNC	

A/D Converters

Table 33: A/D Converter Port Assignment

Signal	Source	I/O Port	Notes
AD4	7709A/7729	AN4/PTL4	
AD5	7709A/7729	AN5/PLT5	
AD6	7709A/7729	AN6/DA0/PLT6	This port can also be used as a DA output.

Sensor Input Ports

Table 34: Sensor Input Port Resource Assignment

Signal	Source	Input Port	Notes
SENIN0	HD64465	PC0	R/O
SENIN1	HD64465	PC1	R/O
SENIN2	HD64465	PC2	R/O
SENIN3	HD64465	PC3	R/O
SENIN4	HD64465	PC4	R/O
SENIN5	HD64465	PC5	R/O
SENIN6	HD64465	PC6	R/O
SENIN7	HD64465	PC7	R/O

This pins could be assigned as R/W however any write functions are typically assigned to the Control I/O port below.

Control I/O Ports

Table 35: Control I/O Port Resource Assignment

Signal	Source	I/O Port	Notes
SENOUT0	HD64465	PA0	R/W
SENOUT1	HD64465	PA1	R/W
SENOUT2	HD64465	PA2	R/W
SENOUT3	HD64465	PA3	R/W
SENOUT4	HD64465	PA4	R/W
SENOUT5	HD64465	PA5	R/W

SENOUT6	HD64465	PA6	R/W
SENOUT7	HD64465	PA7	R/W

Smart Card Interface

Table 36: Smart Card Port Assignment

Signal	Source	I/O Port	Notes
SH_SCRXD	7709A/7729	RXD0/SCPT0	
SH_SCTXD	7709A/7729	TXD0/SCPT0	
SH_SCCLC	7709A/7729	SCK0/SCPT1	

Four Wire Touch Screen Input

Table 37: Four-Wire Touch Screen Resource Assignment

Signal	Source	I/O Port	Notes
GPIO3	HD64465	PE2	Output
GPIO2	HD64465	PE1	Output
GPIO1	HD64465	PE0	Output
TSPX	HD64465	TSPX	Analog Input
TSMX	HD64465	TSMX	Analog Input
TSPY	HD64465	TSPY	Analog Input
TSMY	HD64465	TSMY	Analog Input

Miscellaneous Resource Assignments

Table 38: Miscellaneous Resource Assignments

Signal	Source	I/O Port	Notes
EXP_INT	7709A/7729	PTC7/PINT7	Daughterboard, optional interrupt
LED0	7709A/7729	PTE7	Output; Rev 4 only
PCMCIAEN	7709A/7729	PTH6	Input; Rev 4 or less bd. only
RSTO#	7709A/7729	PTH5/ADTRG#	Input
ASEBRKAK#	7709A/7729	ASEBRKAK#	Input – JTAG function
ASEMDO	7709A/7729	ASEMDO/PTG6	Input – JTAG function
FLWREN	7709A/7729	PTD2/RESOUT#	Output: “1” enable writing of the FLASH
PRST#	7709A/7729	WAKEUP#/PTD3	Software Reset: Normally float. When driven “0” will force system reset
TDO	7709A/7729	TDO/PTE0	JTAG support function; output
AUDSYNC#	7709A/7729	PTE7	AUD Output; Rev 5 Bd. or greater only
AUDCK	7709A/7729	PTH6	AUD Output; Rev 5 Bd. or greater only
AUDATA0	7709A/7729	PTG0	AUD Output; Rev 5 Bd. or greater only
AUDATA1	7709A/7729	PTG1	AUD Output; Rev 5 Bd. or greater only
AUDATA2	7709A/7729	PTG2	AUD Output; Rev 5 Bd. or greater only
AUDATA3	7709A/7729	PTG3	AUD Output; Rev 5 Bd. or greater only

TP	HD64465	PE[4..7]	I/O

Test Point Definitions

TP4	IRQOUT-	7709A/7729	
TP1	PTC7/PINT7	7709A/7729	
TP8	PTE7	7709A/7729	
TP6	PTG4	7709A/7729	
TP7	PTH5/ADTRG	7709A/7729	
TP5	IOC9	V320	
TP3	IOC4	V320	
TP2	IOC1	V320	
TP23	AFECKE	HD64465	
TP	UCKE	HD64465	

Interrupt Assignments

The interrupts on the SH7709A/7729 are assigned as follows:

Table 39: SH7709A/7729 Interrupt Assignments

7709A/7729 Interrupt Input	Source	Signal	Active State	Notes
IRQ0	V320	USC_INT#	Low	Not to be used at present
IRQ1	HD64465	HD65IRQ#	Low	
IRQ2	MQ-200	HD64IRQ#	Low	
IRQ3	CPCI Bus	ENUM#	Low	Indicates a HOT Swap has taken place on the backplane
IRQ4	Ethernet Controller	ENETINT	High	
PINT0	CPCI Bus	INTP	High	
PINT1	CPCI Bus	INTS	High	
PINT2	CPCI Bus	INTA#	Low	
PINT3	CPCI Bus	INTB#	Low	
PINT4	CPCI Bus	INTC#	Low	
PINT5	CPCI Bus	INTD#	Low	
PINT6	CPCI Bus	DEG#	Low	Indicates Power is degrading on CPCI backplane
PINT7	Daughter Board Support	EXP_INT	Undefined	
PINT8	AutoPC Interrupt conn.	AUTOINT0	Low	
PINT9	AutoPC Interrupt conn.	AUTOINT1	Low	

PINT10	AutoPC Interrupt conn.	AUTOINT2	Low	
PINT11	AutoPC Interrupt conn.	AUTOINT3	Low	
PINT12	AutoPC Interrupt conn.	AUTOINT4	Low	
PINT13	AutoPC Interrupt conn.	AUTOINT5	Low	
PINT14	AutoPC Interrupt conn.	AUTOINT6	Low	
PINT15	AutoPC Interrupt connector.	AUTOINT7	Low	

Hardware Initialization Requirements

- SDRAM address mux. timing should be setup identical on the V320 versus SH7709A/7729
- SH3 should float the SDRAM bus when not bus master

HD64465 Area: Area 4

2.Bus width: Longword (32 bits) size and Little Endian access.
3.Idle state: No idle cycles
4.Wait state: **2** wait states

SH7709A/7729 Mode Selections

The following mode selections are hard-wired on the board (except MD3/4).

Table 40: SH7709A/7729 Mode selections

Mode Bit	Function	Setting	Logic Level
MD2/1/0	Clock Setup	Int. Clk.= 4x Ext. Clk.	111
MD4/MD3	Word Size of Address Area 0	Boot selectable between 8 and 32 bits. Determined by Switch SW1 in conjunction with CPLD.	8 = 01 32 = 11
MD5	Little/Big Endian	Little Endian	1

RS-232 Ports

SCIF Port	Definition
RXD1/SCPT2	DTR (software controlled)
SCK1/SCPT3	CD (software controlled)
RxD2/SCPT4	Receive data (console, port 1)
TxD2/SCPT4	Transmit data (console, port 1)

SCI Port	Definition
RxD0/SCPT0	Receive data (console, port 0)
TxD0/SCPT0	Transmit data (console, port 0)

SCIF Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Serial mode register 2	SCSMR2	R/W	H'00	H'4000150	8 bits
Bit rate register 2	SCBRR2	R/W	H'FF	H'4000152	8 bits
Serial control register 2	SCSCR2	R/W	H'00	H'4000154	8 bits
Transmit FIFO data register 2	SCFTDR2	W	Write only	H'4000156	8 bits
Serial status register 2	SCSSR2	R/(W)	H'0060	H'4000158	16 bits
Receive data FIFO register 2	SCFRDR2	R	Undefined	H'400015A	8 bits
FIFO control register 2	SCFCR2	R/W	H'00	H'400015C	8 bits
FIFO data count set register 2	SCFDR2	R	H'0000	H'400015E	16 bits

SCI Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Serial mode register	SCSMR	R/W	H'00	H'FFFFFE80	8 bits
Bit rate register	SCBRR	R/W	H'FF	H'FFFFFE82	8 bits
Serial control register	SCSCR	R/W	H'00	H'FFFFFE84	8 bits
Transmit data register	SCFTDR	W	H'FF	H'FFFFFE86	8 bits
Serial status register	SCSSR	R/(W)	H'84	H'FFFFFE88	8 bits
Receive data register	SCFRDR	R	H'00	H'FFFFFE8A	8 bits
Port SC data register	SCPDR	R/W	H'00	H'4000136	8 bits
Port SC control register	SCPCR	R/W	H'A888	H'4000116	16 bits

Note: For more information, refer to the *SH7709A/7729 Hardware Manual*, Serial Communication Interface with FIFO (SCIF).

Key West Interrupts Operation

There are 21 sources of external interrupts on the Key West Board. The status of any of these external interrupts can be seen by viewing the Interrupt Status Register **ISTAT**, and the Interrupt Mask Register **IMASK**. **ISTAT** contains the present status of the interrupt sources, and **IMASK** is a writeable register which determines whether an interrupt source is masked (default) or unmasked.

Appendix A Key West Bill of Material (BOM)

This will is listed on the CD that can be obtained after signing the Agreement included in the Shipping box.

Appendix B Tahoe PCB Bill of Material (BOM)

This is listed on the CD that can be obtained after signing the Agreement included in the Shipping box.

Appendix C SH7709A/7729 Registers

The following is a detailed description of the SH3 registers used to initialize the processor at power-up/reset time.

Bus Control Register 1 (BCR1)

Bus control register 1 (BCR1) is a 16-bit read/write register that sets the functions and bus cycle state for each area. It is initialized to H'0000 by a power-on reset, but is not initialized by a manual reset or by standby mode. Do not access external memory outside area 0 until BCR1 register initialization is complete.

Bus control register 1 BCR1 H'FFFFFF60 0x0008

bit15:	Pin A25 to A0 not Pulled-Up	(0)
bit14:	Pin D31 to D0 not Pulled-Up	(0)
bit13:	Hi-Z Memory Control	(0)
bit12:	High-Z Control	(0)
bit11:	Endian Flag	(x)
bit10-9:	Area 0 normal ROM	(0 0)
bit8:	Area 5 normal Memory	(0)
bit7:	Area 5 normal Memory	(0)
bit6-5:	Area 6 normal memory	(0 0)
bit4:	Area 2 normal, Area 3 SDRAM Memory	(0)
bit3-2:	Area 2 normal, Area 3 SDRAM Memory	(1 0)
bit1:	Area 5 normal memory	(0)
bit0:	Area 6 normal memory	(0)

Bus Control Register 2 (BCR2)

The bus control register 2 (BCR2) is a 16-bit read/write register that selects the bus-size width of each area. It is initialized to H'3FFC by a power-on reset, but is not initialized by a manual reset or by standby mode. Do not access external memory outside area 0 until BCR2 register initialization is complete.

Bus control register 2 BCR2 H'FFFFFF62 0x3ff0

bit15-14:	Reserved: read as 0.	(0 0)
bit13-12:	Area 6 32-bit Bus Size	(1 1)
bit11-10:	Area 5 32-bit Bus Size	(1 1)
bit9-8:	Area 4 32-bit Bus Size	(1 1)
bit7-6:	Area 3 32-bit Bus Size	(1 1)
bit5-4:	Area 2 32-bit Bus Size	(1 1)
bit3-0:	Reserved: read as 0.	(0 0 0 0)

Wait State Control Register 1 (WCR1)

Wait state control register 1 (WCR1) specifies the idle time between area changes and a read to a write in the same area.

Wait state control register 1 WCR1 H'FFFFFF64 0x3cf3

bit15:	WAIT Sampling at rising edge of CKIO	(0)
bit14:	Reserved: read as 0.	(0)
bit13-12:	Area 6 Intercycle Idle = 3	(1 1)
bit11-10:	Area 5 Intercycle Idle = 3	(1 1)
bit9-8:	Area 4 Intercycle Idle = 0	(0 0)
bit7-6:	Area 3 Intercycle Idle = 3	(1 1)
bit5-4:	Area 2 Intercycle Idle = 3	(1 1)
bit3-2:	Reserved: read as 0.	(0 0)
bit1-0:	Area 0 Intercycle Idle = 3	(1 1)

Wait State Control Register 2 (WCR2)

Wait state control register 2 (WCR2) is a 32-bit read/write register that specifies the number of wait state cycles inserted for each area. It also specifies the pitch of data access for burst memory accesses. This allows direct connection of even low-speed memories without an external circuit. WCR2 is initialized to H'FFFFFFFF by a power-on reset. It is not initialized by a manual reset or by standby mode.

Wait state control register 2 WCR2 H'FFFFFF66 0xfd7e

bit15-13:	A6W	- CS6 wait control: 10 states	(1 1 1)
bit12:	A5W	- CS5 wait control: 10 states	(1)
bit11-10:	A5W	- CS5 wait control: 10 states	(1 1)
bit9-8:	A4W	- CS4 wait control: 2 states	(0 1)
bit9:	A4W	- CS4 wait control: 2 states	(0)
bit6-5:	A3W	- CS3 SDRAM CAS latency: 3 states	(1 1)
bit4:	A2W	- CS2 wait control: 3 states	(1)
bit3:	A2W	- CS2 wait control: 3 states	(1)
bit2-0:	A0W	- CS0 wait control: 8 states	(1 1 0)

Individual Memory Control Register (MCR)

The individual memory control register (MCR) is a 16-bit read/write register that specifies RAS and CAS timing and burst control for DRAM (area 3 only), SDRAM (areas 2 and 3), specifies address multiplexing, and controls refresh. This enables direct connection of DRAM and SDRAM without external circuits.

The MCR is initialized to H'0000 by power-on resets, but is not initialized by manual resets or standby mode. The bits TPC1–TPC0, RCD1–RCD0, TRWL1–TRWL0, TRAS1–TRAS0, RASD, BE, SZ, AMX1–AMX0, and EDOMODE are written to at the initialization after a power-on reset and are not then modified again. When RFSH and RMODE are written to, write the same values to the other bits. When using DRAM, and SDRAM, do not access areas 2 and 3 until this register is initialized.

Individual memory control MCR H'FFFFFF68 0xd72c

```
bit15-14:   RAS Precharge Time = 4 cycles                  ( 1 1     )
bit13-12:   RAS-CAS Delay = 2 cycles                       (     0 1 )
bit11-10:   Write-Precharge Delay = 2 cycles               ( 0 1     )
bit9-8:     CAS -Before-RAS Refresh RAS Assert Time = 4 cyc (     1 1 )
bit7:       Auto precharge                                 ( 0       )
bit6:       Burst Disabled                                 (   0     )
bit5-4:     Address Multiplex 8Mx8                         (     1 0 )
bit3:       Address Multiplex 8Mx8                         ( 1       )
bit2:       Refresh Control                                (   1     )
bit1:       CAS before RAS refresh                         (     0   )
bit0:       normal SDRAM                                   (       0 )
```

SDRAM Mode Register (SDMR3)

The synchronous DRAM mode register (SDMR3) is a write-only virtual 16-bit register that is written to via the synchronous DRAM address bus, and sets the mode of the area 3 synchronous DRAM.

SDRAM Mode Register SDMR3 0x8C0

Refresh Timer Control/Status Register (RTSCR)

Refresh timer control/status register (RTSCR) is a 16-bit read/write register that specifies the refresh cycle, whether to generate an interrupt. It is initialized to H'0000 by a power-on reset, but is not initialized by a manual reset or standby mode.

Note: Writing to the RTCSR differs from that to general registers to ensure the RTCSR is not rewritten incorrectly. Use the word-transfer instruction to set the upper byte as B'10100101 and the lower byte as the write data.

Refresh Timer Control/Status Register RTSCR 0xA50C

Refresh Time Constant Register (RTCOR)

Refresh time constant register (RTCOR) defines the period between each refresh cycle. It is calculated by getting from the SDRAM data sheet the number of refresh cycles to be completed by a certain time frame.

Refresh Time Constant Register RTCOR 0xA5BE

Other Registers

RTCNT	0xA500
RFCR	0xA7C1
BCR3	0x0000
FRQCR	0x0112
DCR	0x0000

Appendix D Key West Jumpers (listed by Function)

Following is a detailed description of the jumper locations on the Key West PCB. The jumpers are listed by function.

Audio/Analog

JP10 Hitachi AFE Adapter (from 465)
JP25 Speaker (miniature connector -- 2 pins) SH7729 AN7/PLT7
JP29 ADC/DAC pins (AN4 to AN7)
JP43 AUD Connector (10 pins)

AutoPC

J12 AutoPC Connector (120 pins)
JP36 AutoPC Interrupt Connector (10 pin DIP)

JP31 AutoPC Interrupt Enable
In = Enable interrupts
Out = Disable

JP39 AutoPC Power Selection **???? Remove jumper for CompactPCI ????**
1-2 = 3.3 volts
2-3 = 5 volts

ATX Power Supply

JP1 ATX Power Connector

JP11 ATX Enable Power
In = Enable
Out = Disable

Big Endian / Little Endian Select

R123 0 ohm resistor/jumper for Big Endian mode
open for Little Endian mode
(7709A/7729 MD5 signal) (bottom side of PCB)

Clocks

JP5 1-2 66 MHz System clock from oscillator
Pin 1 = 66 MHz oscillator output
Pin 2 = Input for external 66 Mhz clock (for debug)
Pin 3 = Gnd

JP6 1-2 33 MHz PCI clock from oscillator
Pin 1 = 33 MHz oscillator output
Pin 2 = Input for external 33 Mhz clock (for debug)
Pin 3 = Gnd

JP8 System Clock Frequency Select
In = 33 MHz
*Out = 66 MHz

JP41 & JP42 Clock Skew
Controls clock skew for:
Sysclk, SDRAM
Off-board clocks.

CPLD Programming Port

JP2 System CPLD (6 pin SIP)
JP30 PCI CPLD (6 pin SIP)

DIP Switches

S1-1
S1-2
S1-3
S1-4

S2-1 SH3's PTL0
S2-2 SH3's PTL1
S2-3 SH3's PTL2
S2-4 SH3's PTL3

Expansion Bus

J10 140 pin connector (Hitachi Tahoe daughter board)
JP37 200 pin connector (Hitachi daughter boards)

JTAG / E10A Interface

JP15 Harp JTAG (JP28) Enable
In = Enable Harp JTAG
Out = Disable Harp JTAG

JP18 JTAG2 Enable PCI Path
In = Enable PCI path
Out = ?

JP21 JTAG3 PCI Bypass
In = PCI Bypass
Out = ?

JP26 Local JTAG
1-2 = Enable local JTAG
2-3 = Bypass

JP27 Hitachi JTAG (14 pin DIP connector)
JP28 Harp JTAG (6 pin)
1 = GND 4 = RST#
2 = TDO 5 = TMS
3 = TDI 6 = CLK

PCI and PCMCIA

J5 & J7 & J11 CompactPCI Connectors

JP7 PCI Clock Frequency Select
In = 16.6 MHz
*Out = 33 MHz

JP35 PCMCIA / PCI Select (for CS5 and CS6 addressing space)
In = PCI
Out = PCMCIA

JP38 CompactPCI System Slot Indicator
In = Standalone
Out = CPCI application

JP40 PCI Boot EEPROM Write Enable
In = Enable write
Out = Disable Flash write

System Flash Memory

JP14 System Flash Write Enable
In = Disable Flash writes
Out = Enable Flash writes

Note: * = default jumper position (if function is implemented)

Appendix E Key West Jumpers (listed by Jumper number)

Following is a list of the jumper locations on the Key West PCB. The jumpers are listed in numerical order.

JP1	Disable Tahoe MQ-200
JP2	System CPLD (6 pin SIP connector)
JP3	N/A
JP4	N/A
JP5	66 MHz System clock source
JP6	33 MHz PCI clock source
JP7	PCI Clock Frequency (16.6/33 MHz)
JP8	System Clock Frequency (33/66 MHz)
JP9	66 MHz clock to Tahoe
JP10	N/A
JP11	ATX Power Supply Enable
JP12	N/A
JP13	N/A
JP14	System Flash Write Enable
JP15	Harp JTAG (JP28) Enable
JP16	N/A
JP17	JTAG – N/A
JP18	JTAG – N/A
JP19	N/A
JP20	N/A
JP21	JTAG PCI Bypass
JP22	N/A
JP23	N/A
JP24	N/A
JP25	Audio output (Miniature connector -- 2 pins)
JP26	Local JTAG Enable
JP27	Hitachi JTAG /E10A (14 pin DIP connector)
JP28	Harp JTAG (6 pin connector)
JP29	ADC/DAC pins (AN4 to AN7)
JP30	PCI CPLD (6 pin SIP connector)
JP31	AutoPC Interrupt Enable
JP32	N/A
JP33	N/A
JP34	N/A
JP35	PCMCIA / PCI Select (for CS5 and CS6 addressing space)
JP36	AutoPC Interrupt Connector (10 pin DIP)
JP37	Expansion connector (200 pins)
JP38	CompactPCI System Slot Indicator
JP39	AutoPC Power Selection
JP40	PCI Boot EEPROM Flash Write Enable
JP41	Clock skew: SDRAM Clk/Companion Chips/Off-board clocks
JP42	Clock skew: SDRAM Clk/Companion Chips/Off-board clocks
JP43	AUD Connector (10 pin)
R123	Big Endian / Little Endian (7709A/7729 MD5 signal) (bottom side of PCB)

External Connectors

J1	ATX Power Connector
J2	Parallel Port Connector (25 pin female)
J3	PS/2 Mouse Connector (5 pin DIN female)
J4	PS/2 Keyboard Connector (5 pin DIN female)

J5	CompactPCI Connector
J6	VGA Connector (15 pin female)
J7	CompactPCI Connector
J8	USB Connector (4 pins)
J9	Serial Debug (9 pin male)
J10	Expansion connector (140 pins)
J11	CompactPCI Connector
J12	AutoPC Connector (120 pins)
T1	RJ45 Ethernet Connector

Appendix F Tahoe Daughterboard Connectors

External Connectors

J1	Line In
J2	Mono Mic In
J3	Amplified headphone out
J4A	PS/2 Keyboard Connector (5 pin DIN female)
J4B	PS/2 Mouse Connector (5 pin DIN female)
J5A	VGA Connector (15 pin female)
J5B	Product RS-232 Serial
J5C	Parallel Port (25 pin female0
J6A	USB (lower)
J6B	USB (upper)
J8	PCMCIA Socket (upper)
J9	PCMCIA Socket (lower)